

Sakhir 10, 10C, 10G

LA-2491 Schematics Document

Intel Dothan / Alviso GM(PM) / DDR-1 / ICH6-M / Fix Bay

(nVIDIA NV43M / NV44M / ATi M22 / M24)

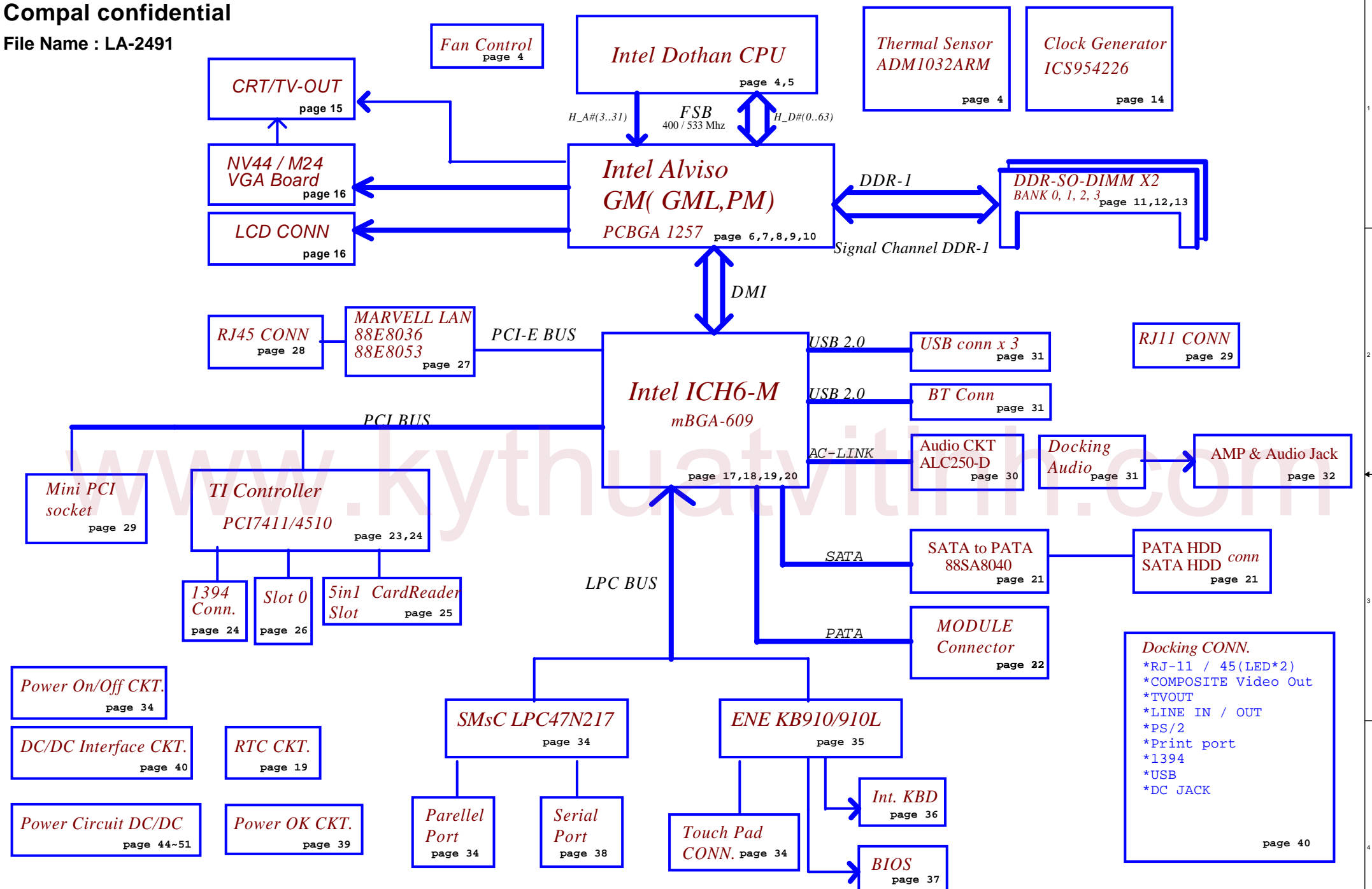
2004 / 12 / 27

Rev:1.A

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File Name : LA-2491



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for Direct CD	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD20	2	PIRQA/PIRQB
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

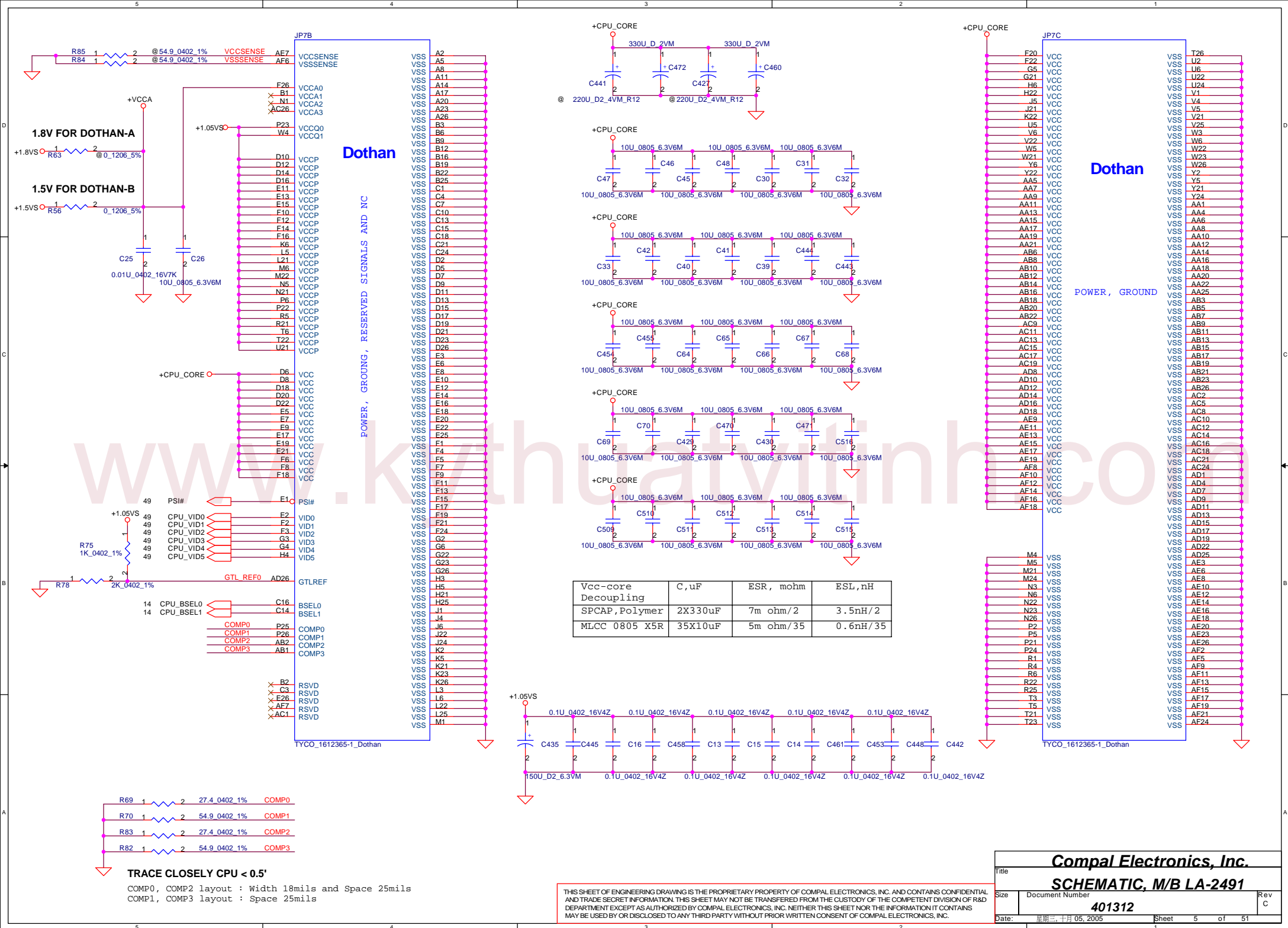
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1.A
5	
6	
7	

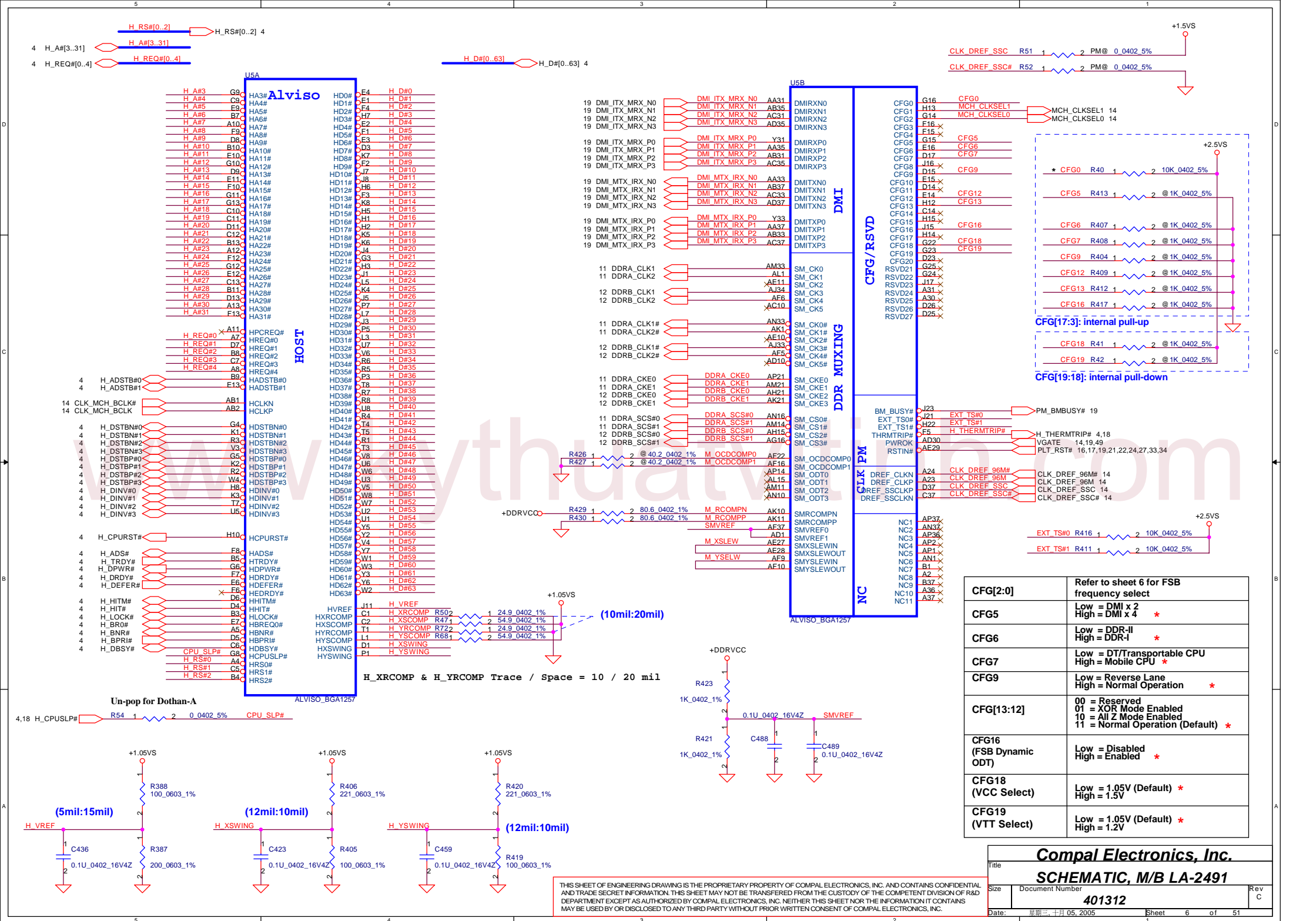
SKU ID Table

SKU_ID_CHECK_0	SKU_ID_CHECK_1	7	6	5
		1-Button	3-Buttons	7-Buttons
0	10	1		0
1	10C	3	12	2
2	10G	5		4
3	10GC	7	13	6
4	10J	11		10
5				
6				

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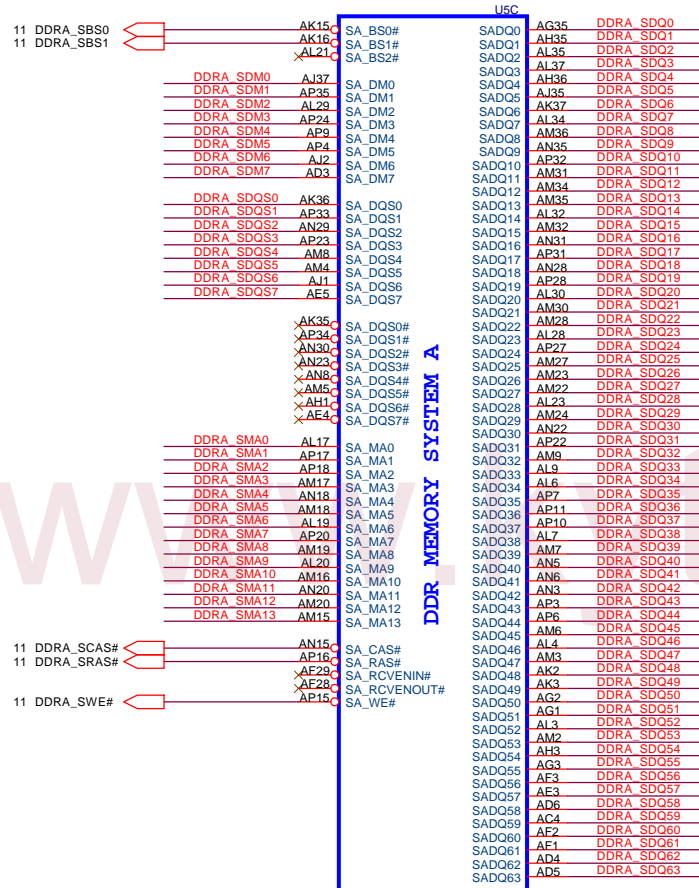
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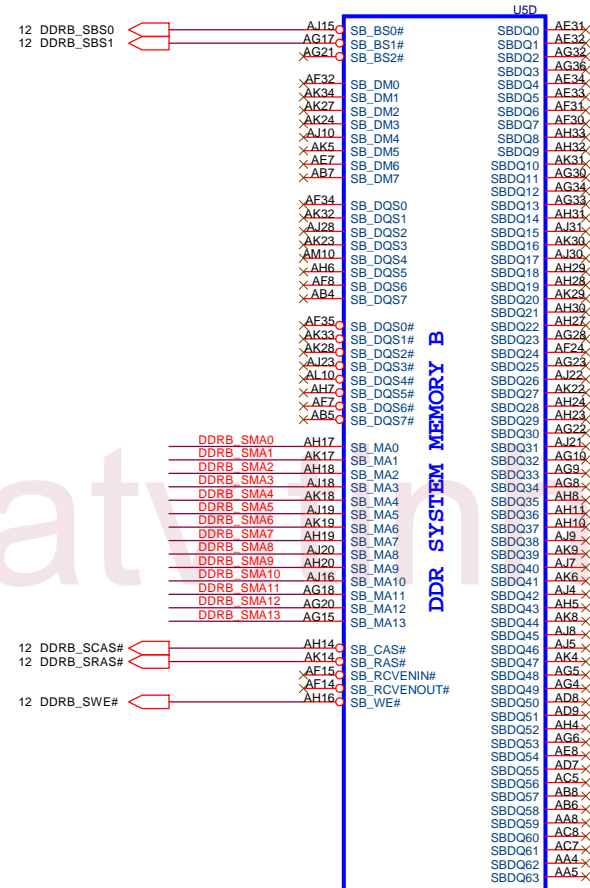


11 DDRA_SDQ[0..63] DDRA_SDQ[0..63]
11 DDRA_SDM[0..7] DDRA_SDM[0..7]
11 DDRA_SDQS[0..7] DDRA_SDQS[0..7]
11 DDRA_SMA[0..13] DDRA_SMA[0..13]

12 DDRB_SMA[0..13] DDRB_SMA[0..13]



ALVISO_BGA1257



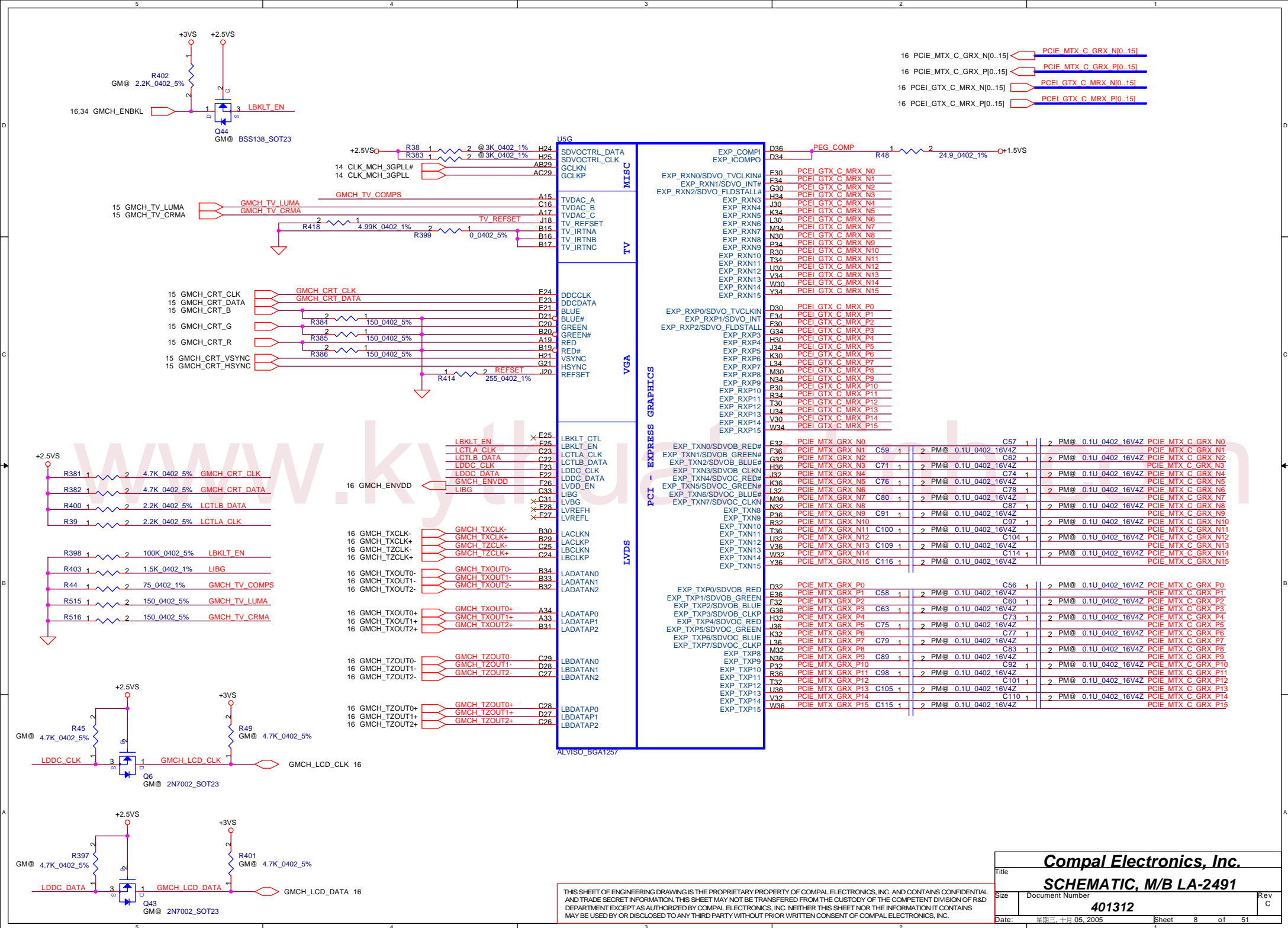
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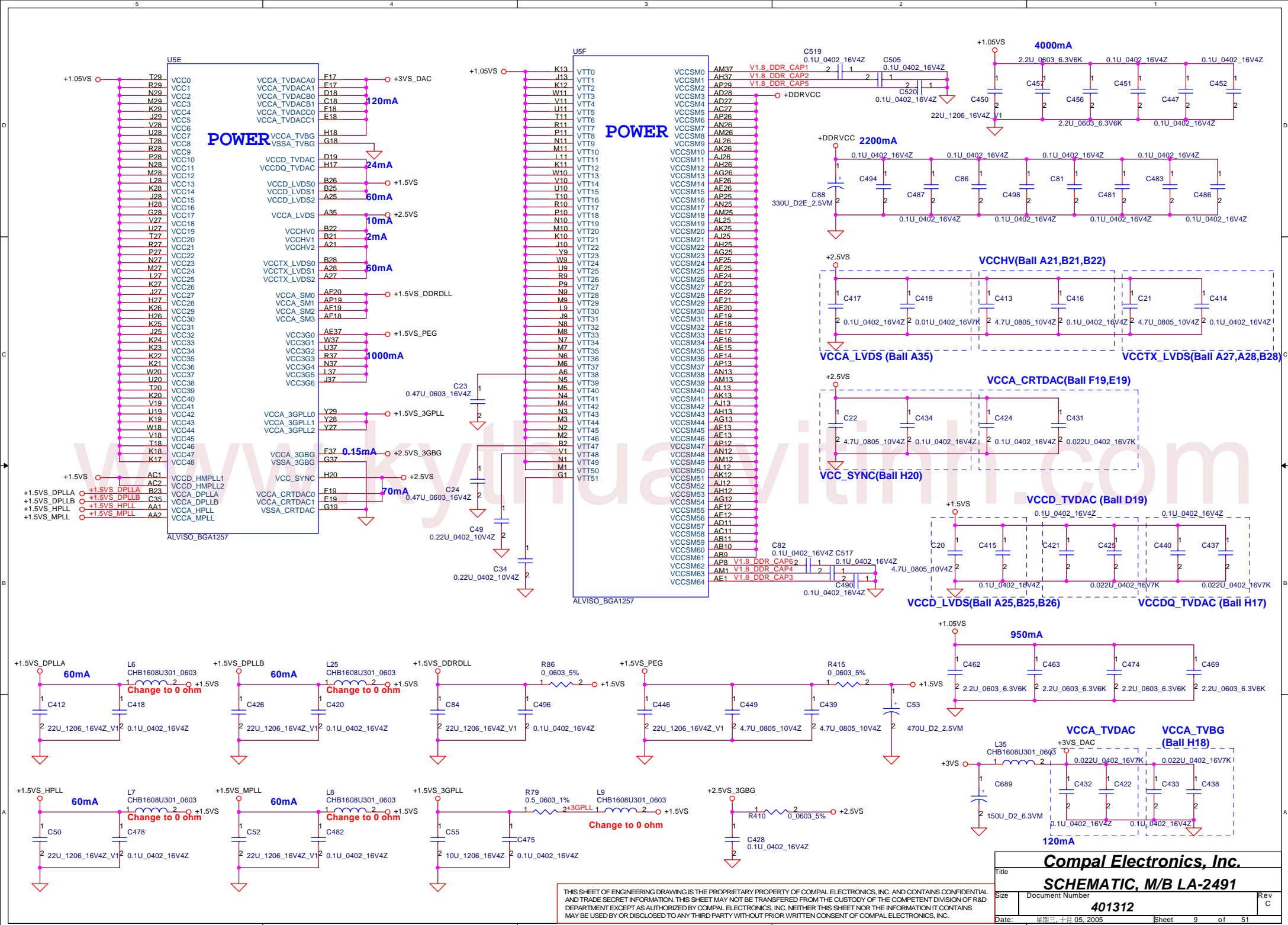
DDR MEMORY SYSTEM A

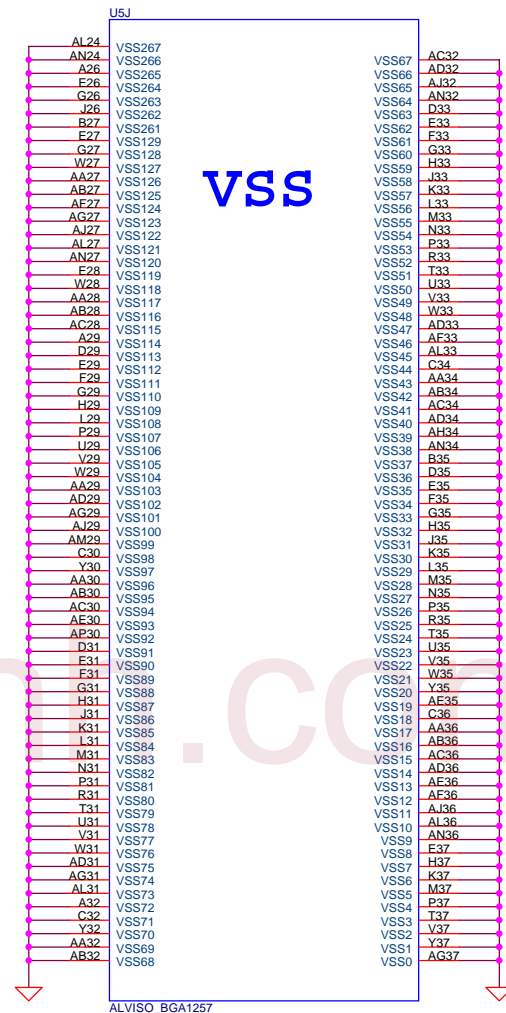
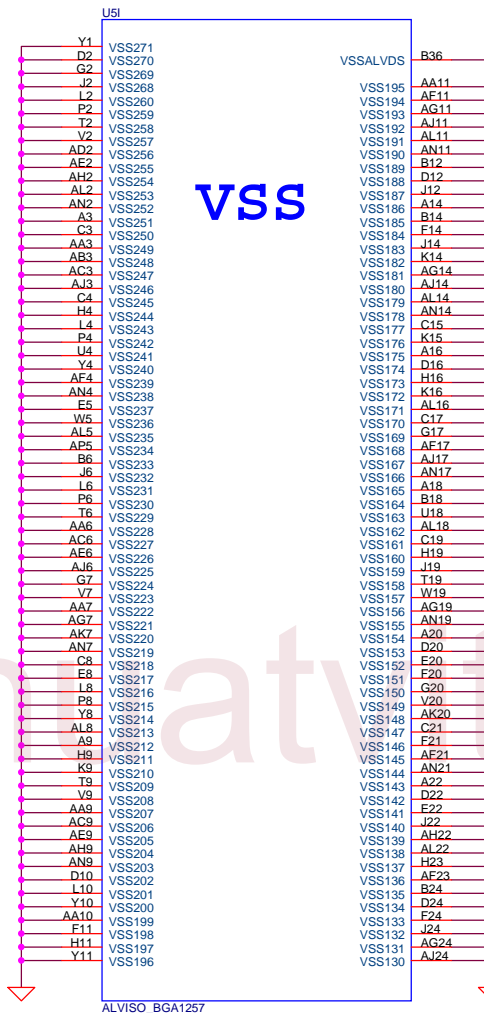
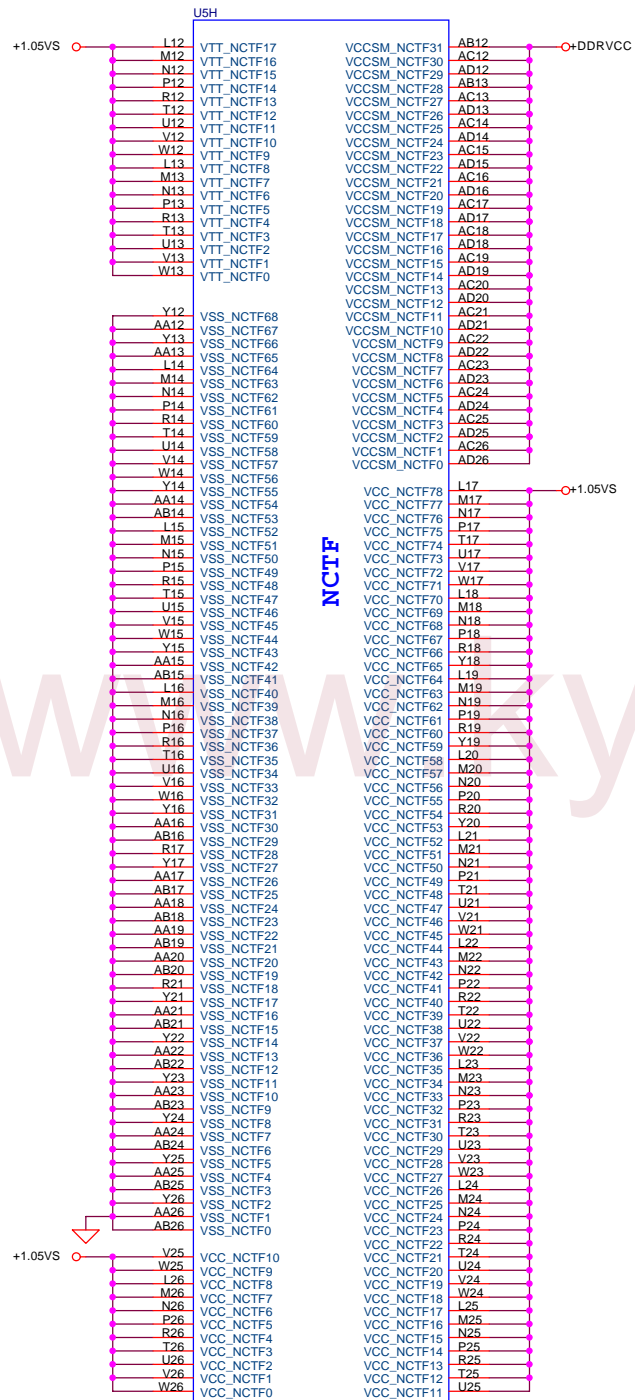
DDR SYSTEM MEMORY B

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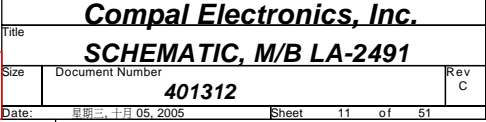


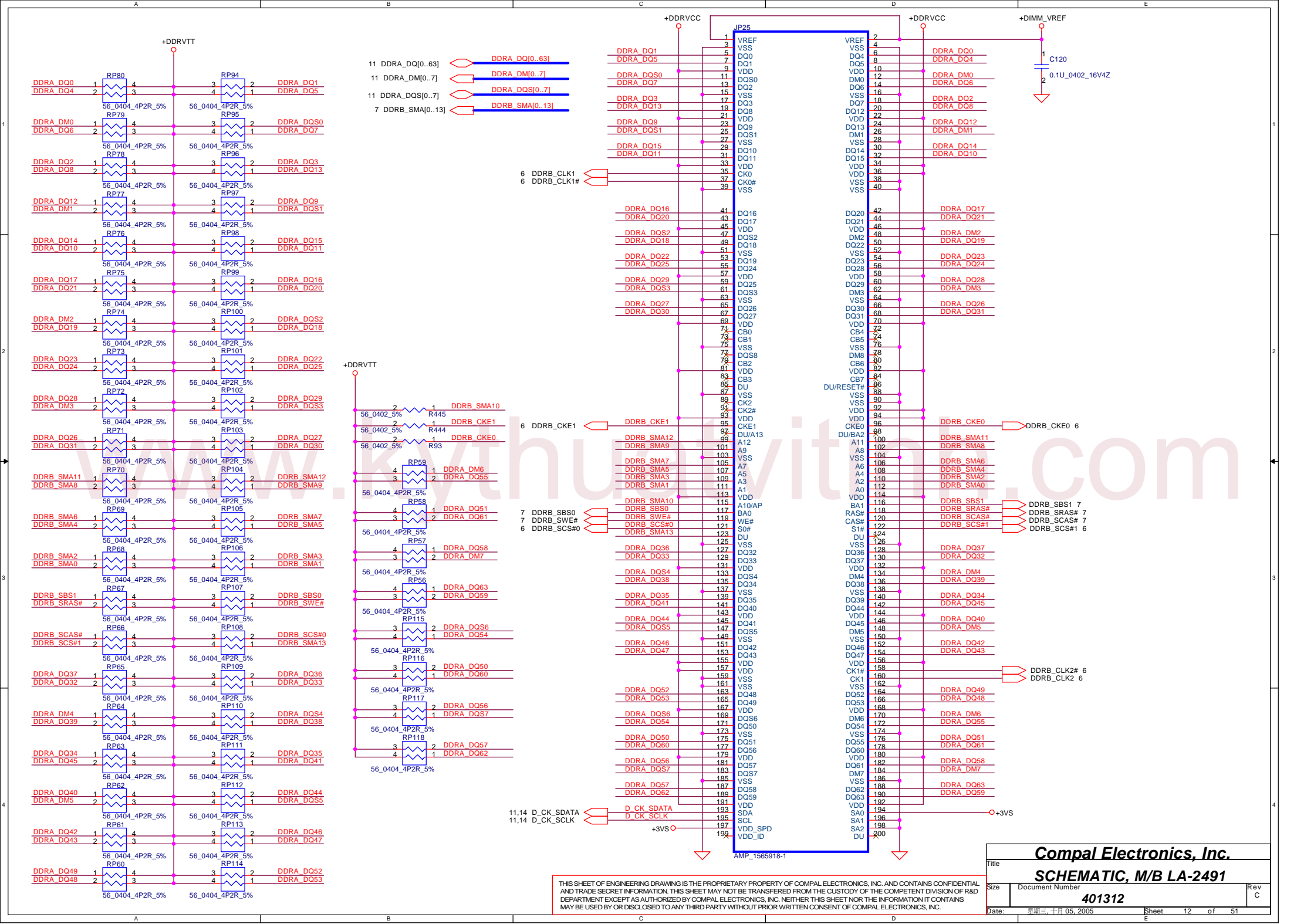




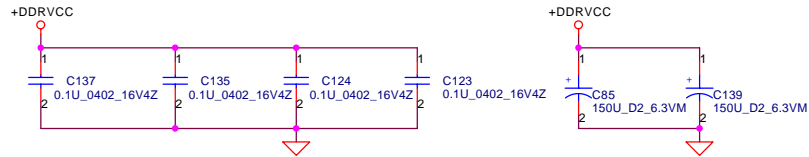
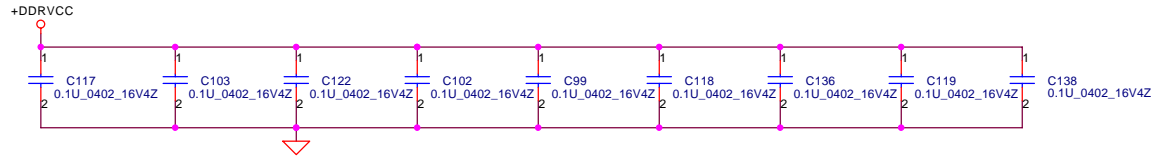
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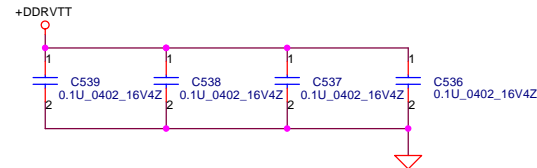
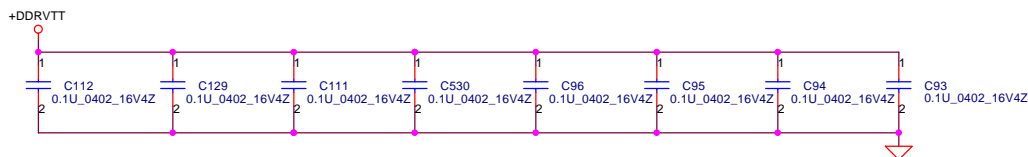
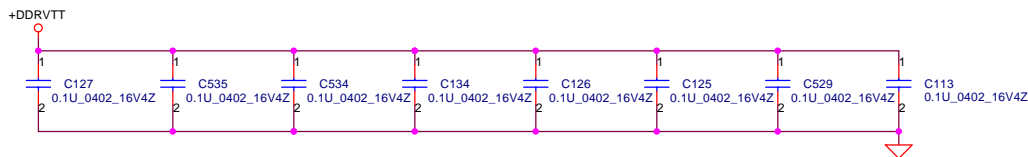
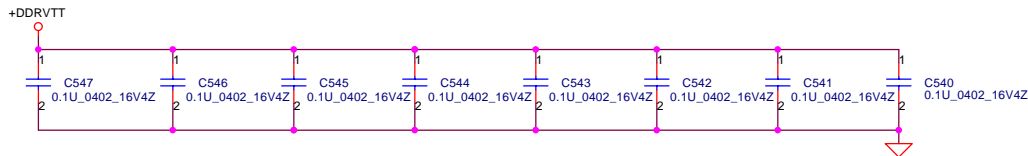
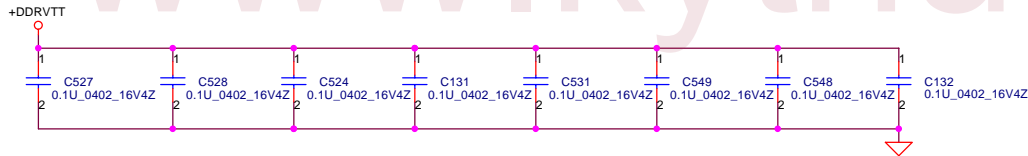
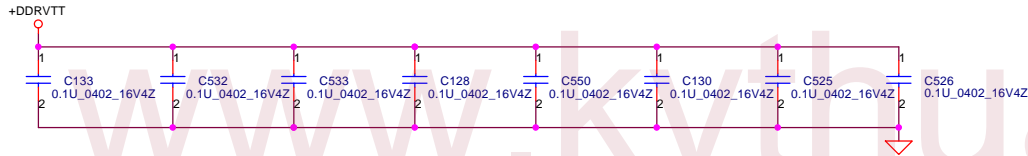




Layout note :
Distribute as close as possible
to DDR-SODIMM.



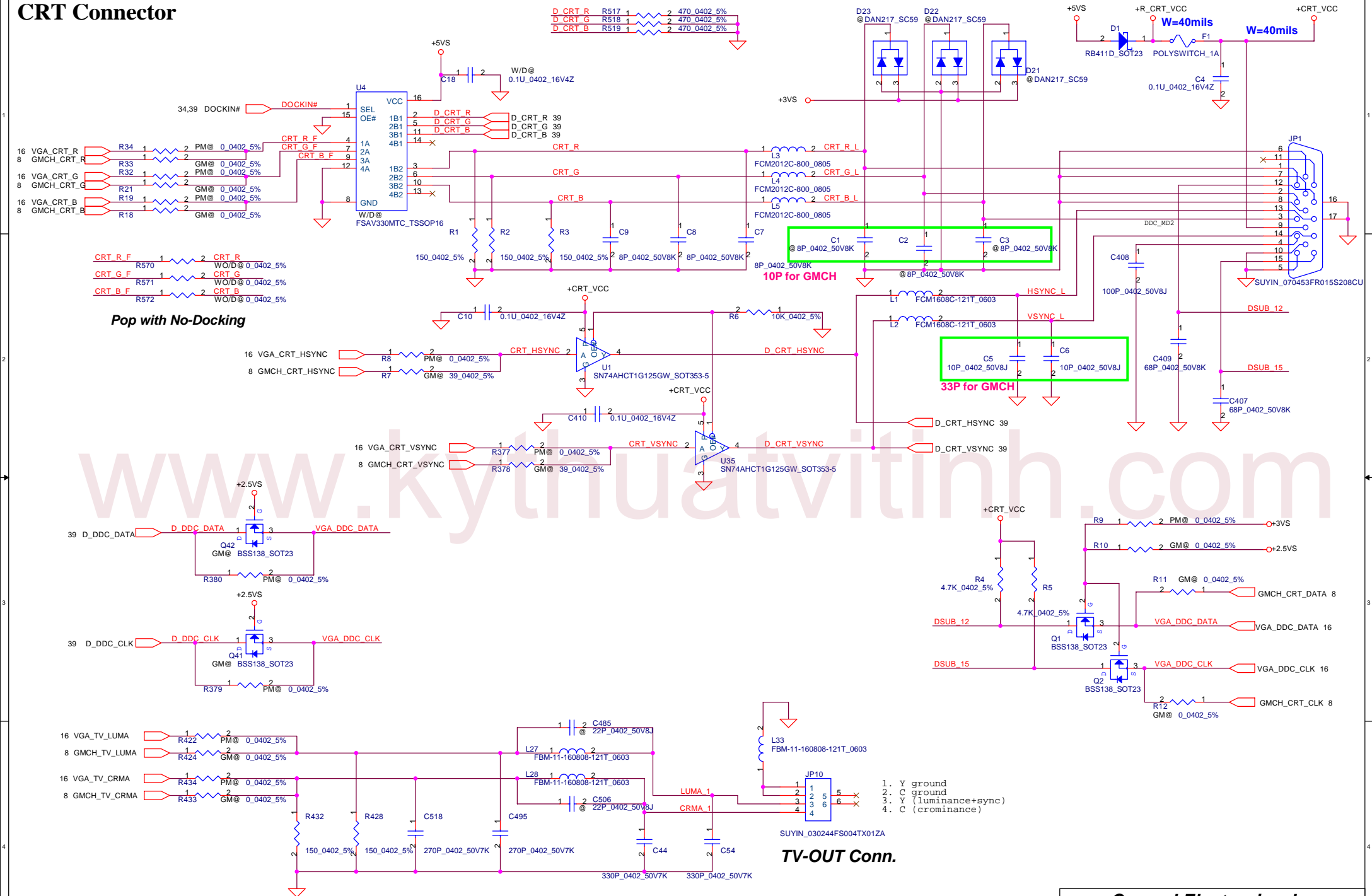
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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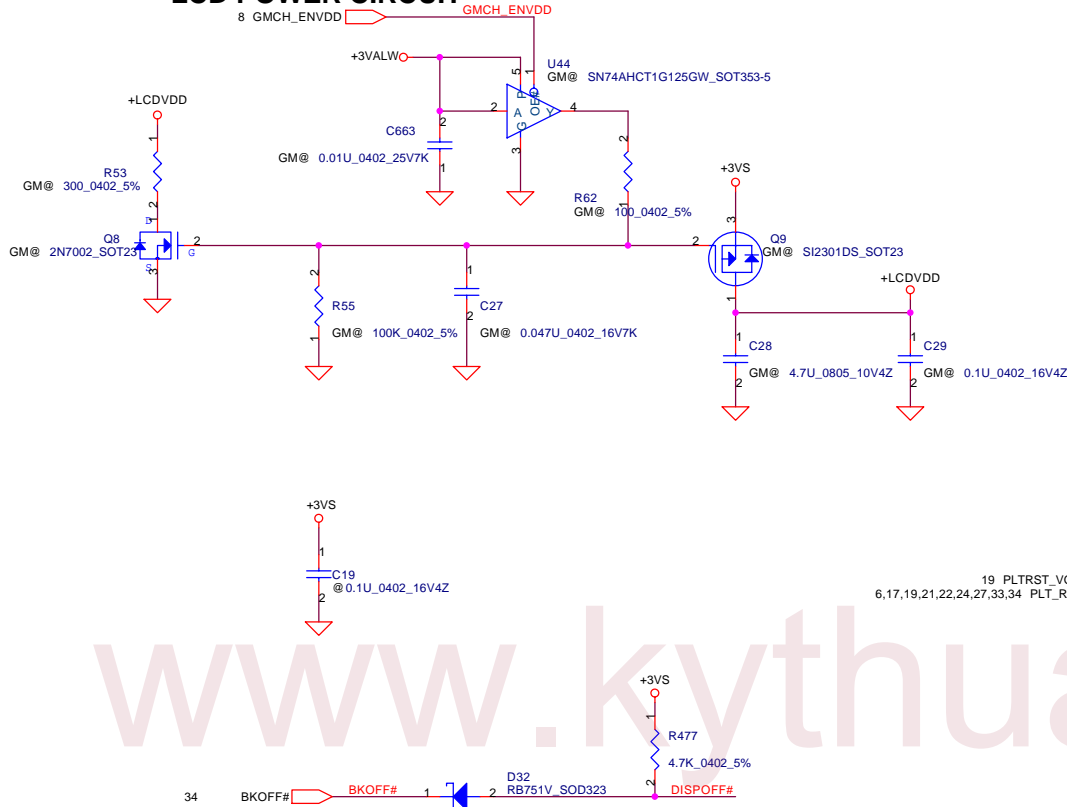
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CRT Connector

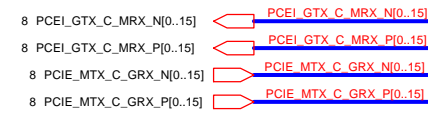
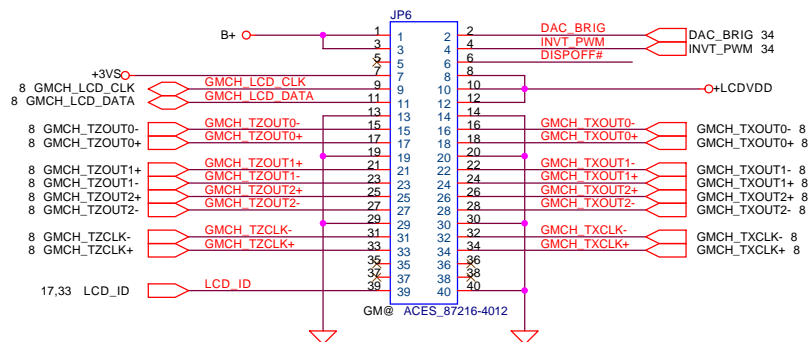


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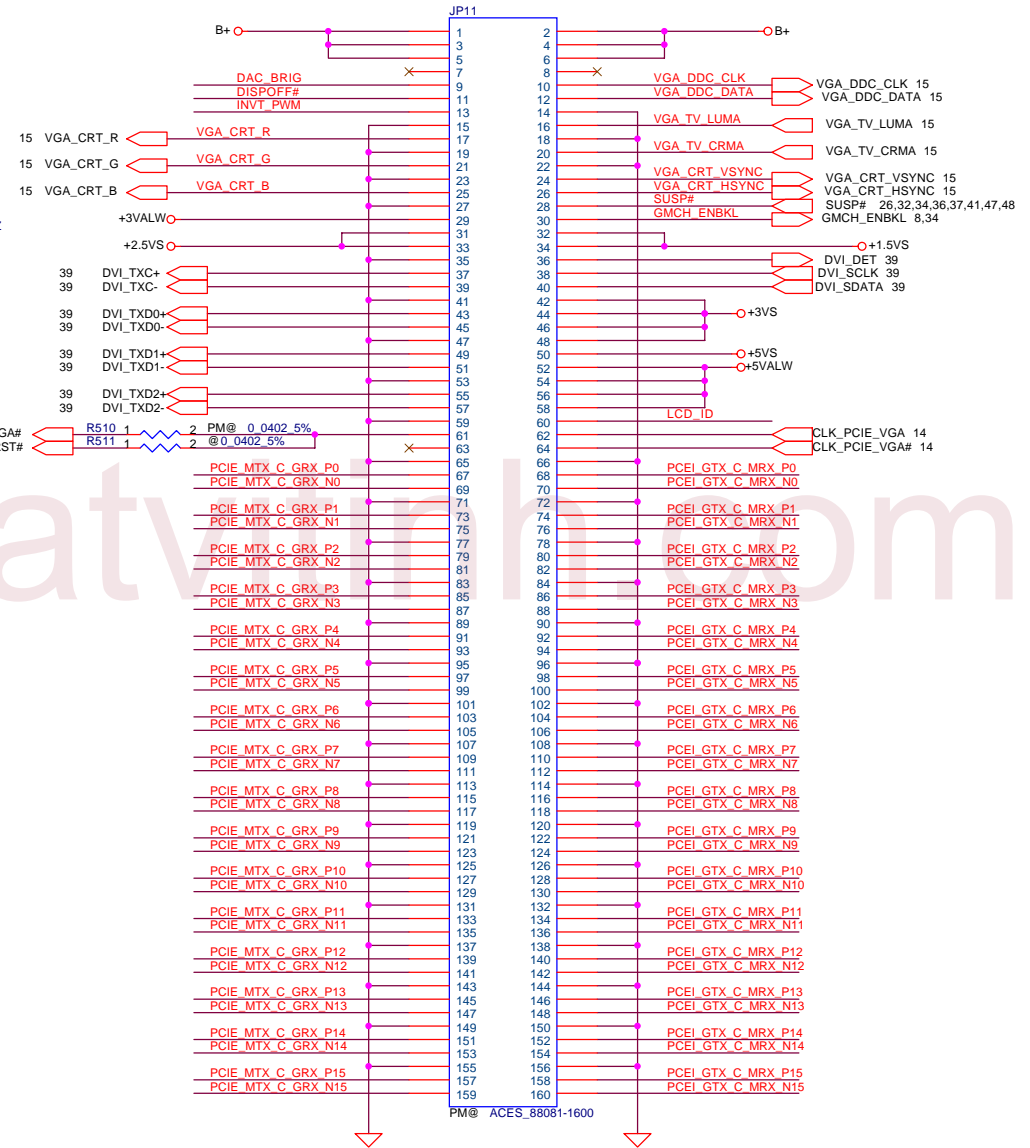
LCD POWER CIRCUIT

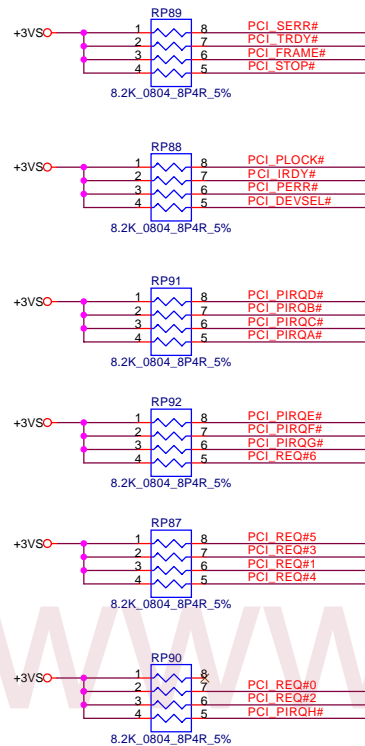


LCD/PANEL BD. Conn.

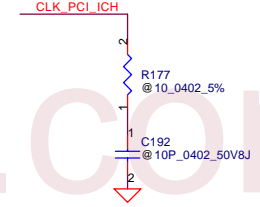
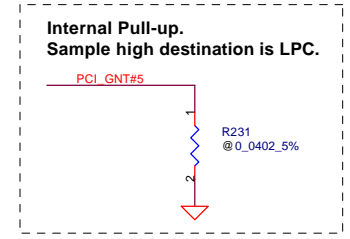
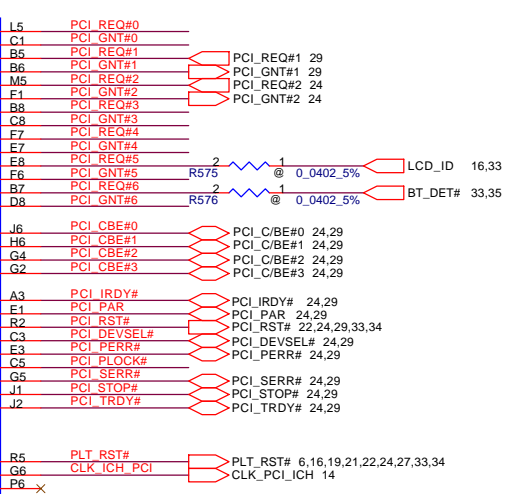
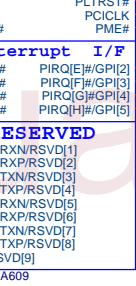
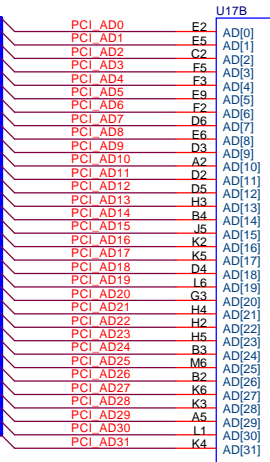


VGA BOARD Conn.



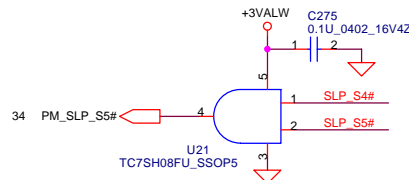
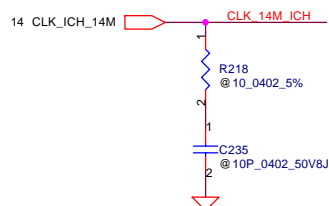
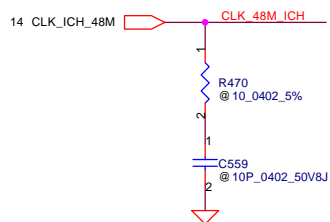
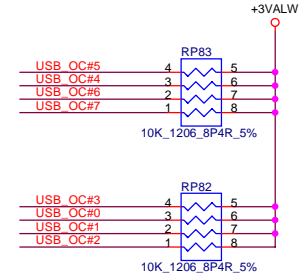
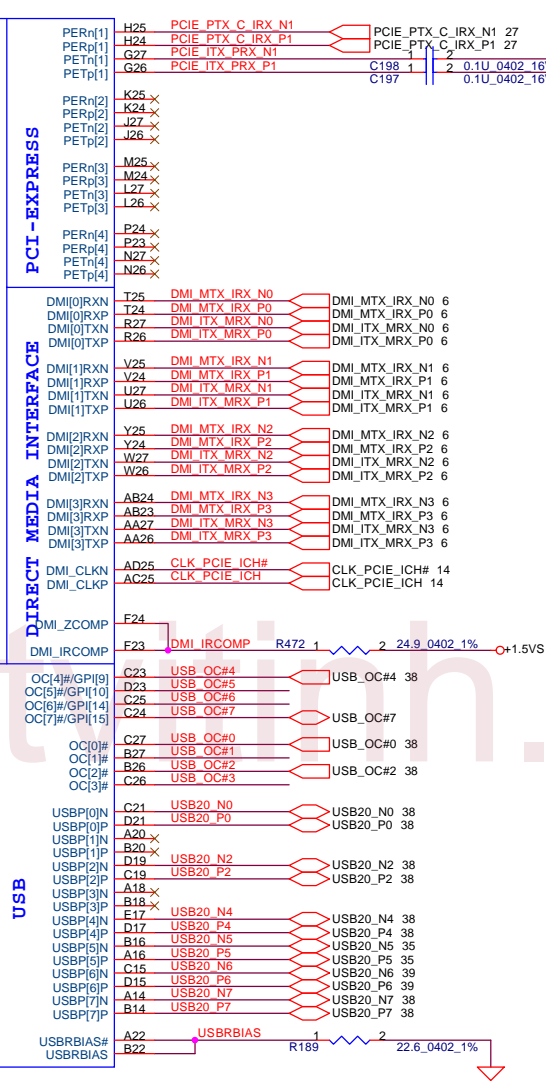
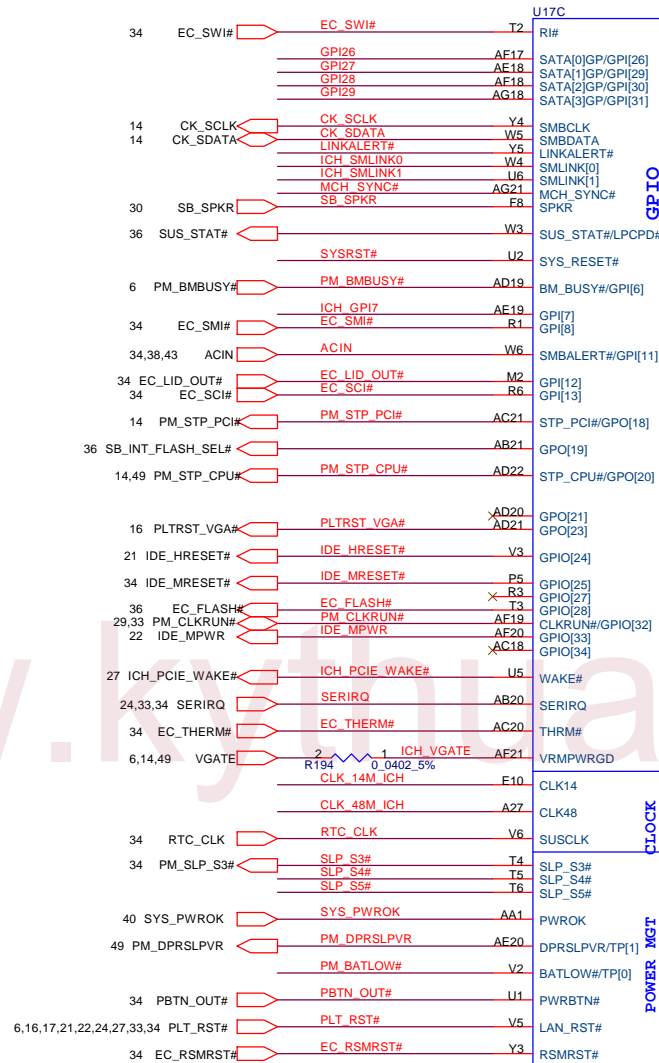
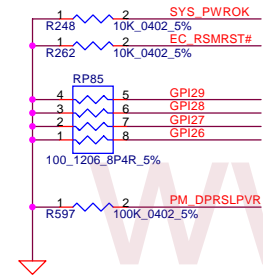
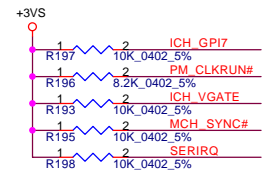
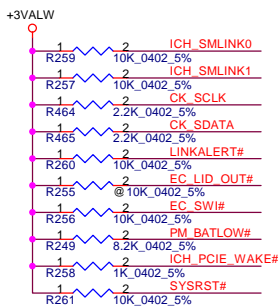


24,29 PCI_AD[0..31]



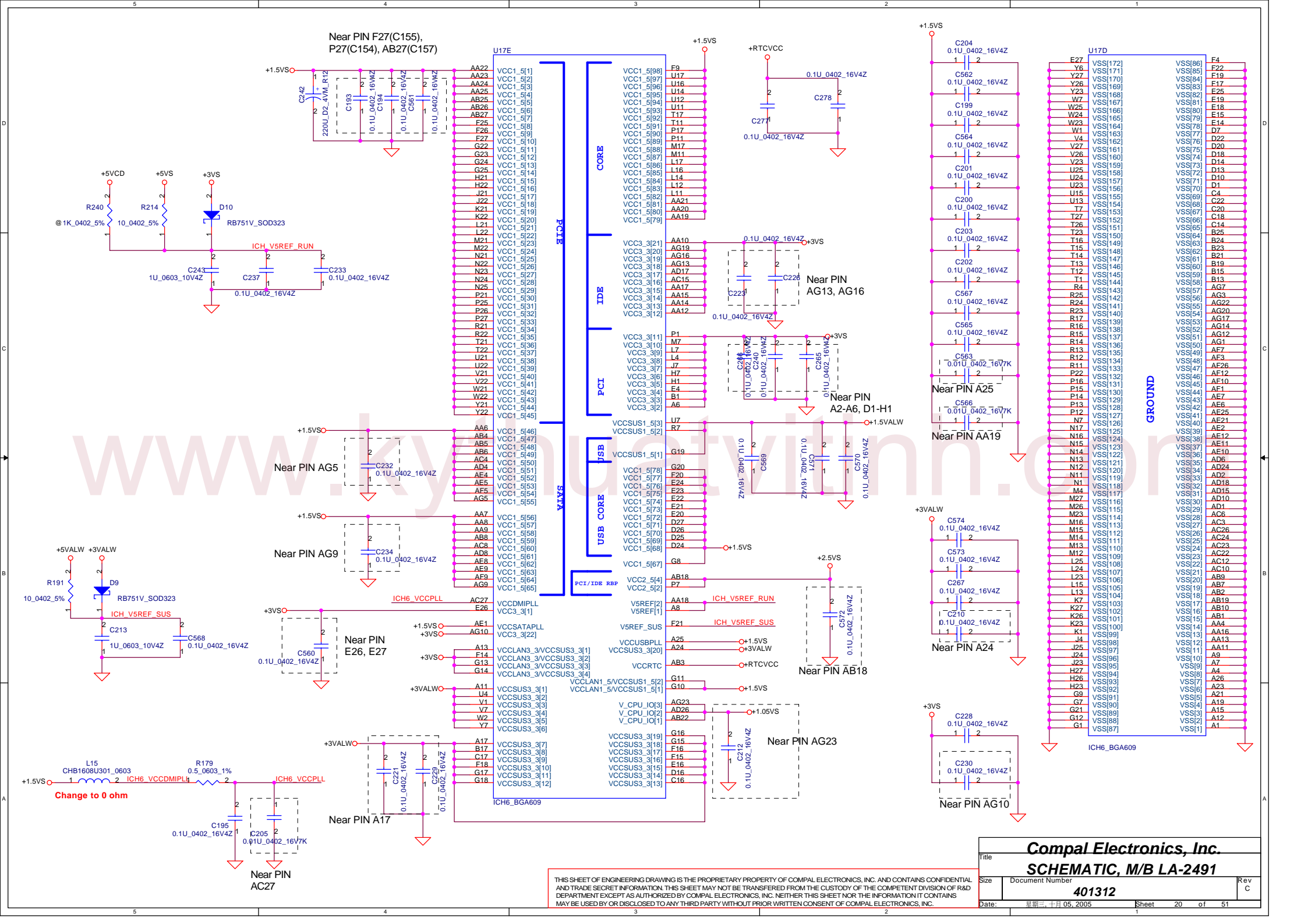
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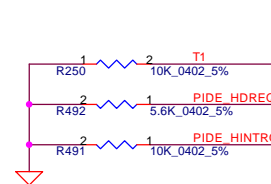
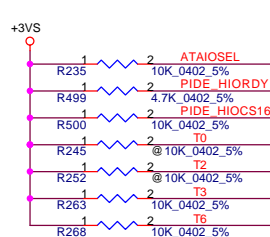
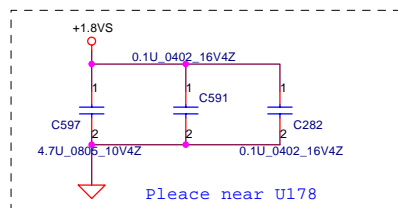
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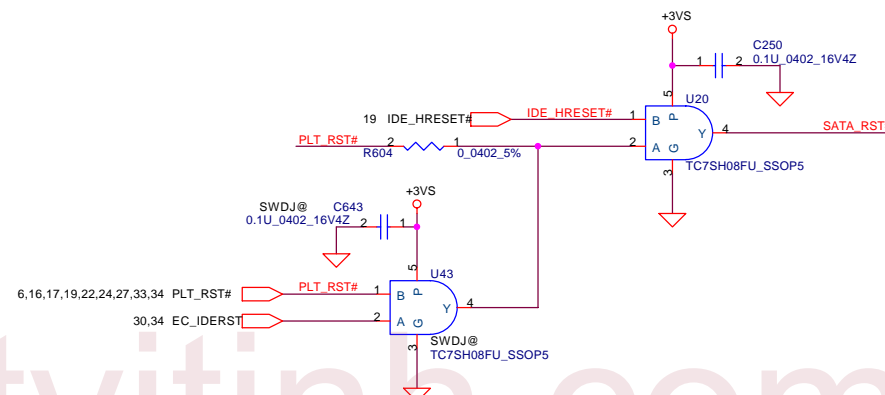
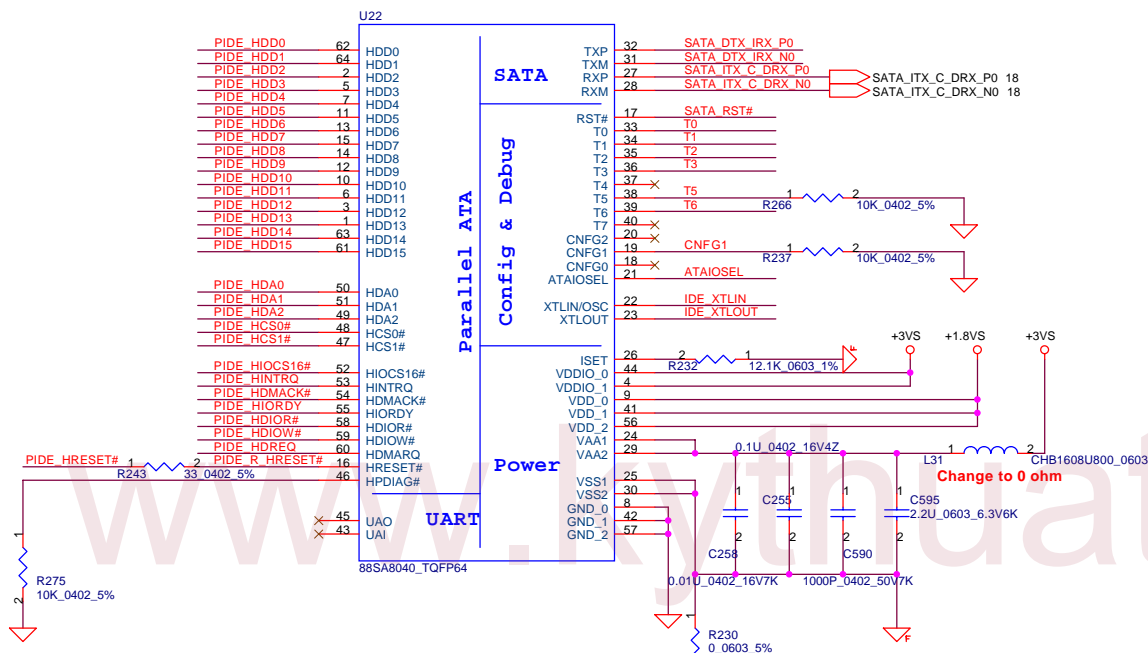
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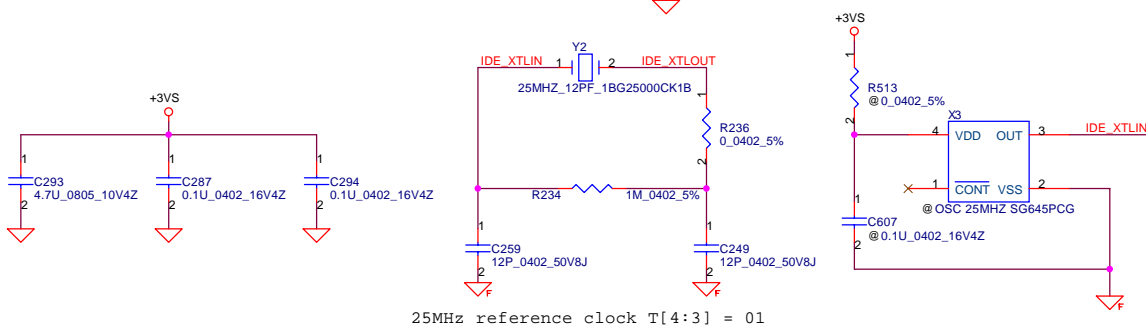


Sets maximum transfer rate and UDMA mode

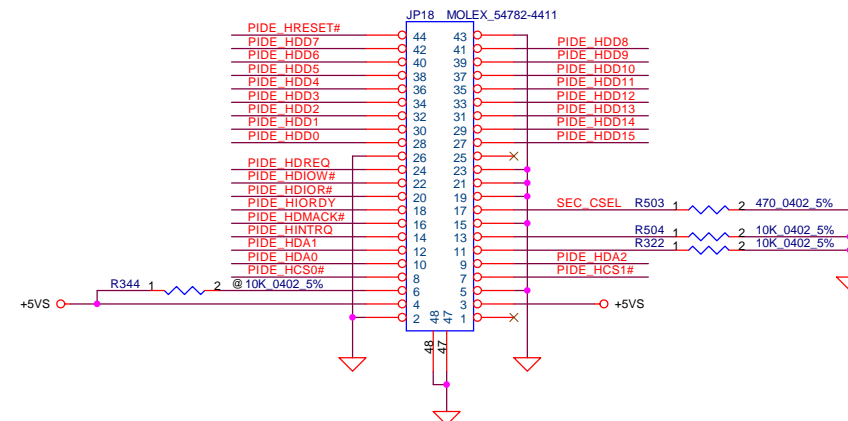
CNFG2 INT PD	CNFG1	CNFG0 INT PD	NOTE
0	0	0	Device Mode 100MB/s
0	0	1	Device Mode 133MB/s
0	1	0	Device Mode 150MB/s
1	0	0	Host Mode 100MB/s
1	0	1	Host Mode 133MB/s
1	1	0	Host Mode 150MB/s
0	1	1	Reserved
1	1	1	Reserved



P-ATA HDD Conn.



```
25MHz reference clock T[4:3] = 01
```

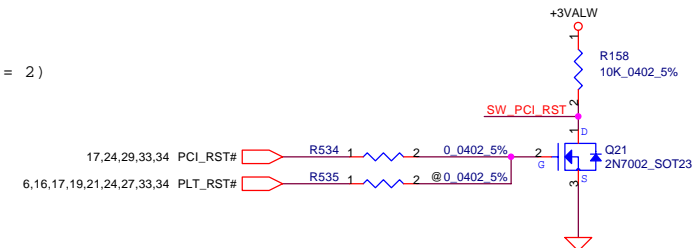
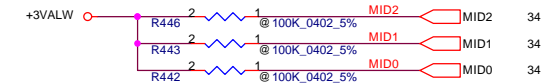
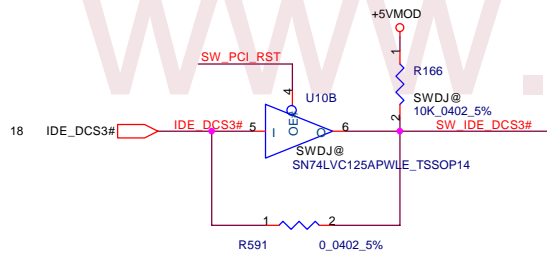


Place near connector side.



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[illegible]**Module Conn.**

26 S1_A[0..25] S1_A[0..25]
26 S1_D[0..15] S1_D[0..15]

S1_D10 D1 A_CAD31/A_D10
S1_D9 C1 A_CAD30/A_D9
S1_D1 D3 A_CAD29/A_D1
S1_D8 C2 A_CAD28/A_D8
S1_D0 B1 A_CAD27/A_D0
S1_A0 A4 A_CAD26/A_A0
S1_A1 A4 A_CAD25/A_A1
S1_A2 E6 A_CAD24/A_A2
S1_A3 B5 A_CAD23/A_A3
S1_A4 C6 A_CAD22/A_A4
S1_A5 B6 A_CAD21/A_A4
S1_A6 G9 A_CAD20/A_A6
S1_A25 C7 A_CAD19/A_A25
S1_A7 B7 A_CAD18/A_A7
S1_A24 A7 A_CAD17/A_A24
S1_A17 A10 A_CAD16/A_A17
S1_IOWR# E11 A_CAD15/A_IOWR#
S1_IORD# G11 A_CAD14/A_A9
S1_IORD# C11 A_CAD13/A_IORD#
S1_OE# B11 A_CAD12/A_A11
S1_CE2# B12 A_CAD11/A_OE#
S1_A10 A12 A_CAD10/A_CE2#
S1_D15 E12 A_CAD8/A_D15
S1_D7 C13 A_CAD7/A_D7
S1_D13 F12 A_CAD6/A_D13
S1_D6 A13 A_CAD5/A_D6
S1_D12 C14 A_CAD4/A_D12
S1_D5 E13 A_CAD3/A_D5
S1_D11 A14 A_CAD2/A_D11
S1_D4 B14 A_CAD1/A_D4
S1_D3 E14 A_CAD0/A_D3

26 S1_REG# S1_REG# C5 A_CCBE3#/A_REG#
S1_A12 F9 A_CCBE2#/A_A12
26 S1_A8 B10 A_CCBE1#/A_A8
26 S1_CE1# G12 A_CCBE0#/A_CE1#

S1_A13 G10 A_CPAR/A_A13
S1_A23 C8 A_CFRAME#/A_A23
S1_A22 A8 A_CTRDY#/A_A22
S1_A15 B8 A_CIRDY#/A_A15
S1_A20 A9 A_CSTOP#/A_A20
S1_A21 C9 A_CDEVEL#/A_A21
S1_A19 E10 A_CBLOCK#/A_A19
S1_A14 F10 A_CPERR#/A_A14
S1_WAIT# B3 A_CSERR#/A_WAIT#
S1_INPACK# E7 A_CREQ#/A_INPACK#
S1_WE# B9 A_CQNT#/A_WE#
S1_BVD1 B2 A_CSTSCHG/A_BVD1(STSCHG/R1)
S1_WP C3 A_CCLKRUN#/A_WP(10IS16)
S1_WP E9 A_CCLK/A_A16
S1_RDY# C4 A_CINT#/A_READY(IREQ)
S1_RST A6 A_CRST#/A_RESET

26 S1_BVD2 S1_BVD2 A2 A_CAUDIO/A_BVD2(SPKR#)

26 S1_CD1# S1_CD1# C15 A_CCD1#/A_CD1#
26 S1_CD2# S1_CD2# E5 A_CCD2#/A_CD2#
26 S1_VS1 S1_VS1 A3 A_CVS1/A_VS1#
26 S1_VS2 S1_VS2 E8 A_CVS2/A_VS2#

+3VS
R305 2 1 10K 0402 5% E2 A_USB_EN#
R304 2 1 10K 0402 5% E1 B_USB_EN#

U41A

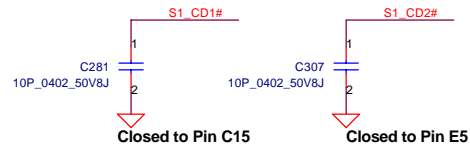
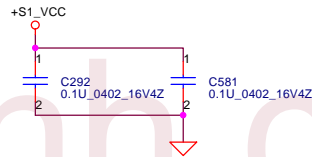
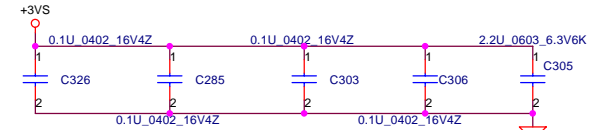
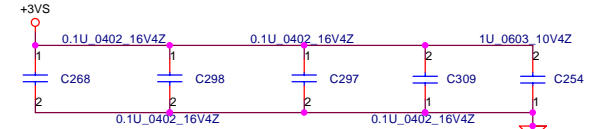
A5 VCCA
A11 VCCA
U8 VCC
U8 H10 VCC
U8 H11 VCC
U8 H12 VCC
U8 J8 VCC
U8 M8 VCC
U8 M9 VCC
U8 M10 VCC
U8 M12 VCC
U8 K8 VCC
U8 K12 VCC
U8 N7 VCC
D19 X
K19 X
RSVD
RSVD

PCI 7411

DATA N1
CLOCK L6
LATCH N2
DATA 26
CLOCK 26
LATCH 26

RSVD B15
RSVD A16
RSVD B16
RSVD A17
RSVD C16
RSVD D17
RSVD C19
RSVD D18
RSVD E17
RSVD E19
RSVD G15
RSVD F18
RSVD H14
RSVD H15
RSVD G17
RSVD K17
RSVD L13
RSVD K18
RSVD L15
RSVD L17
RSVD L18
RSVD L19
RSVD M17
RSVD M14
RSVD M15
RSVD N19
RSVD N18
RSVD N15
RSVD M13
RSVD P18
RSVD P19
RSVD P15
RSVD G18
RSVD K14
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RSVD E18
RSVD J15
RSVD F14
RSVD B18
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RSVD E19
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RSVD A15
RSVD K15

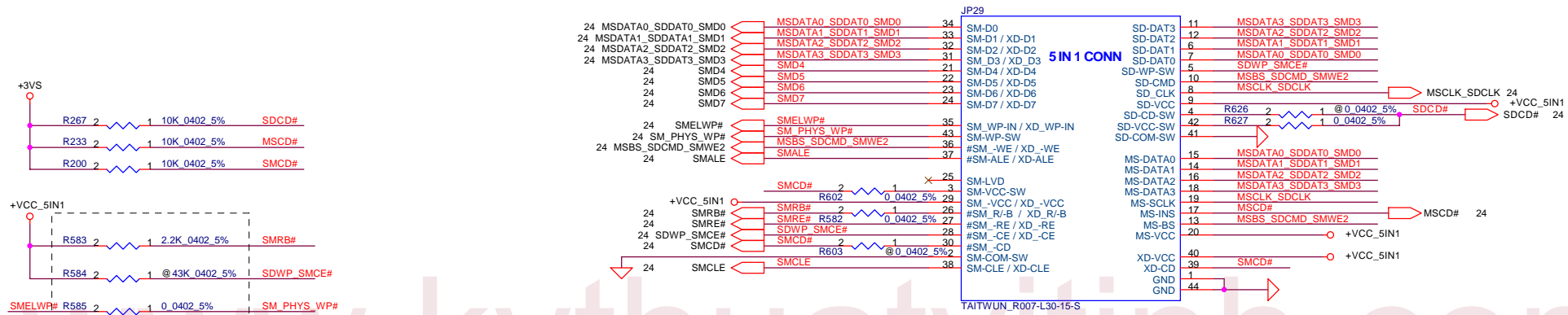
4510 2 2
R579 @ 1K 0402 5%
Reserve for TI PCI4510



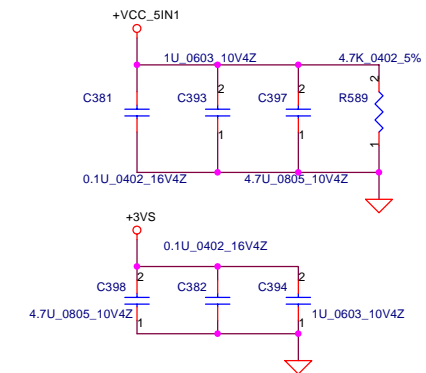
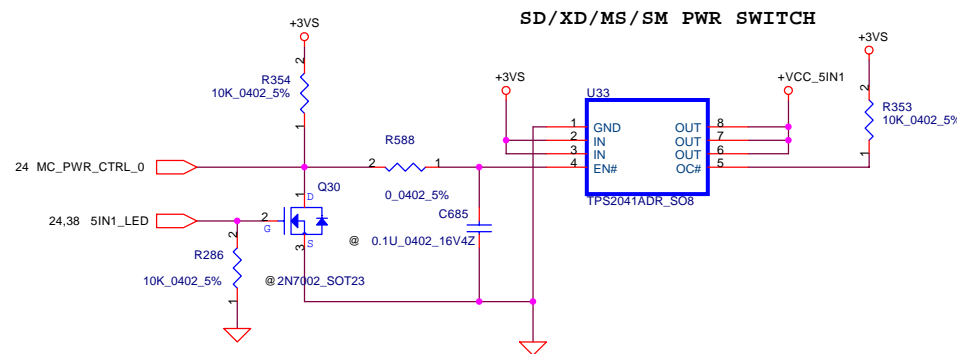
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5 in 1 CardReader Conn.



TI Workaround need check

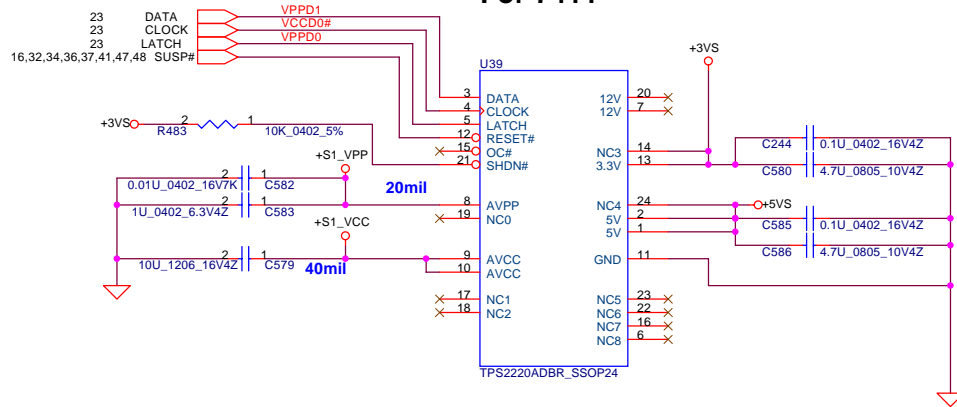


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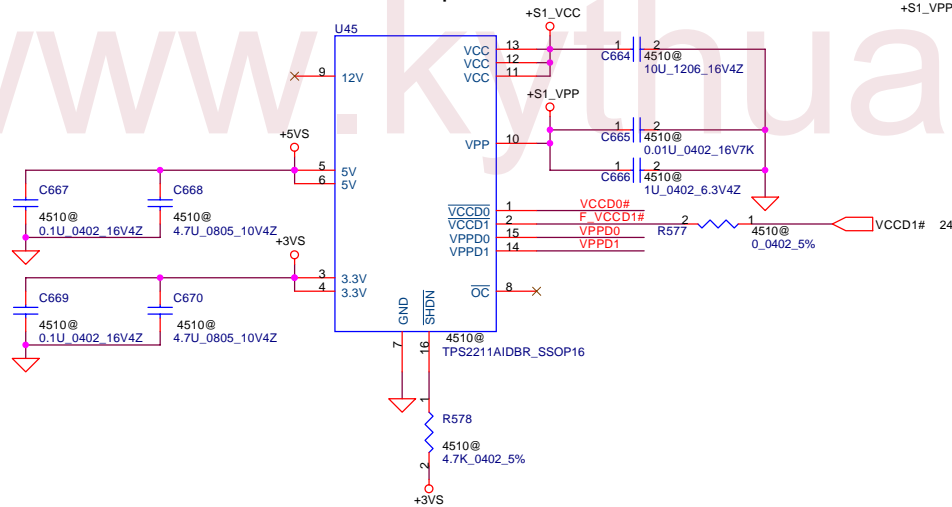
Power Switch for PCMCIA

For 7411

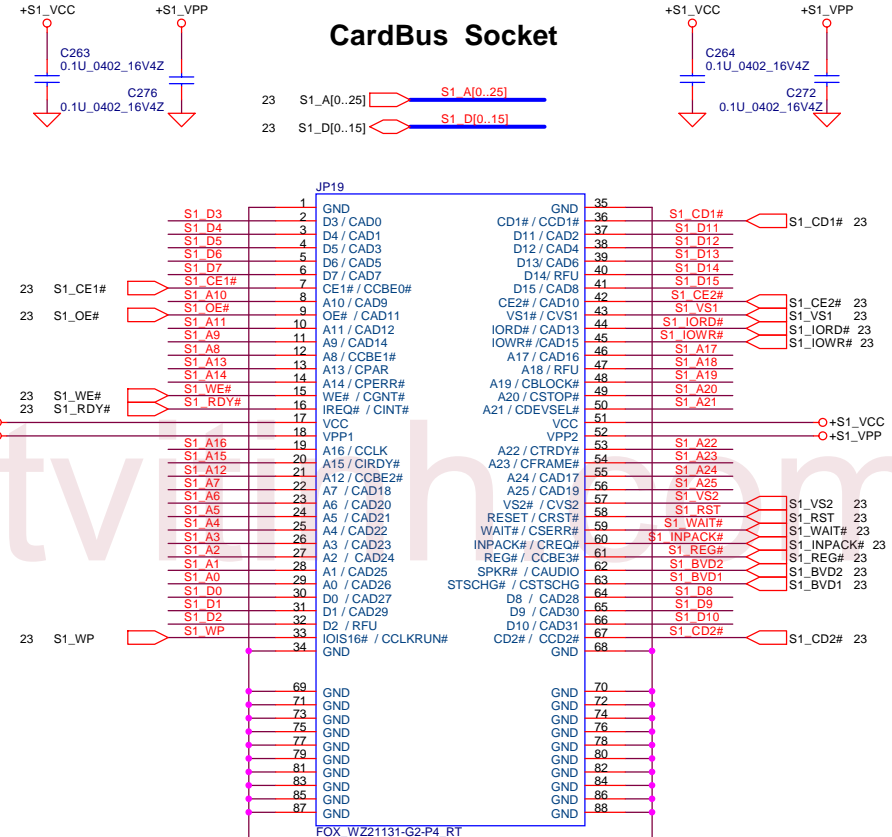


For 4510

use U4 footprint



CardBus Socket

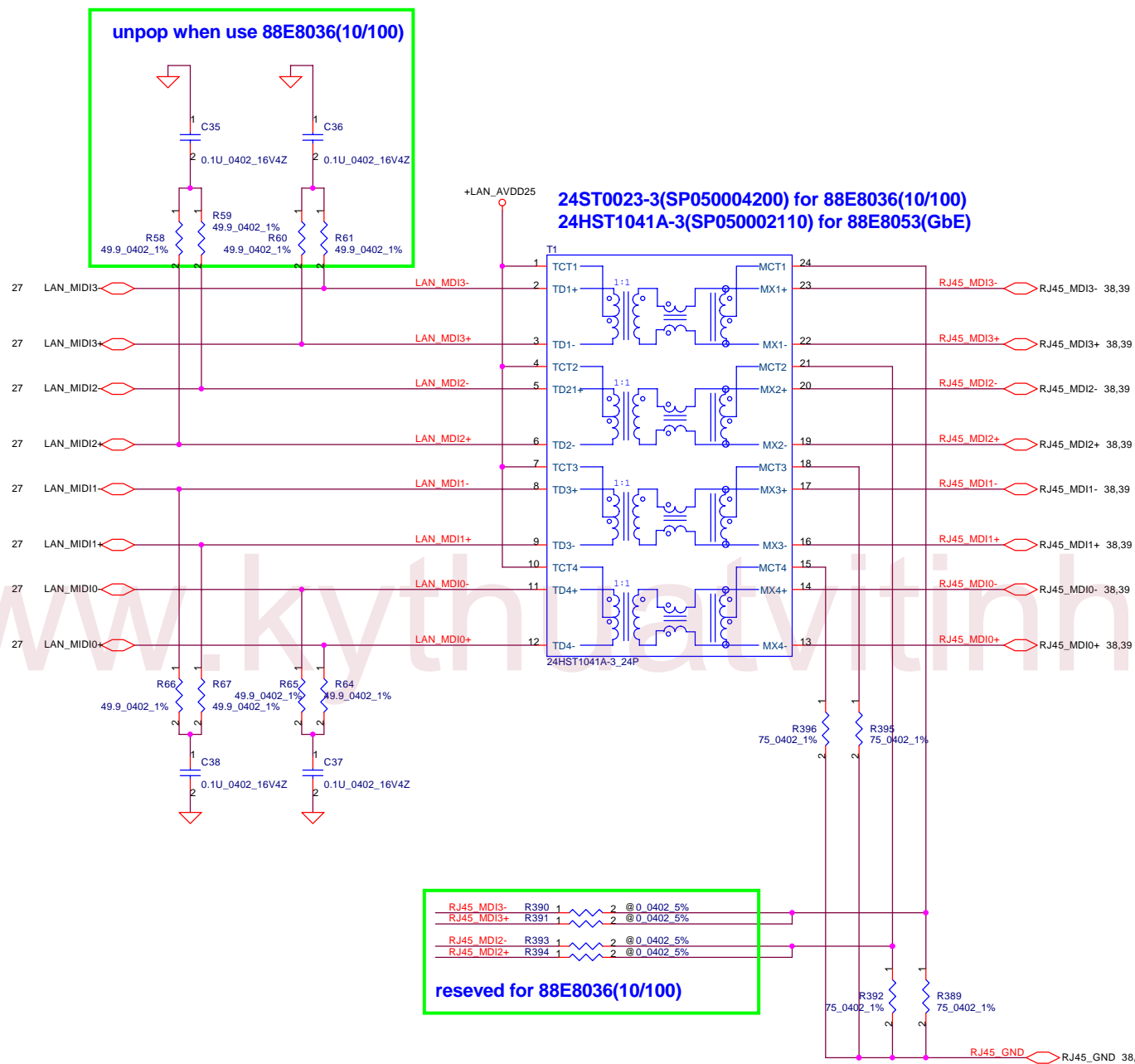


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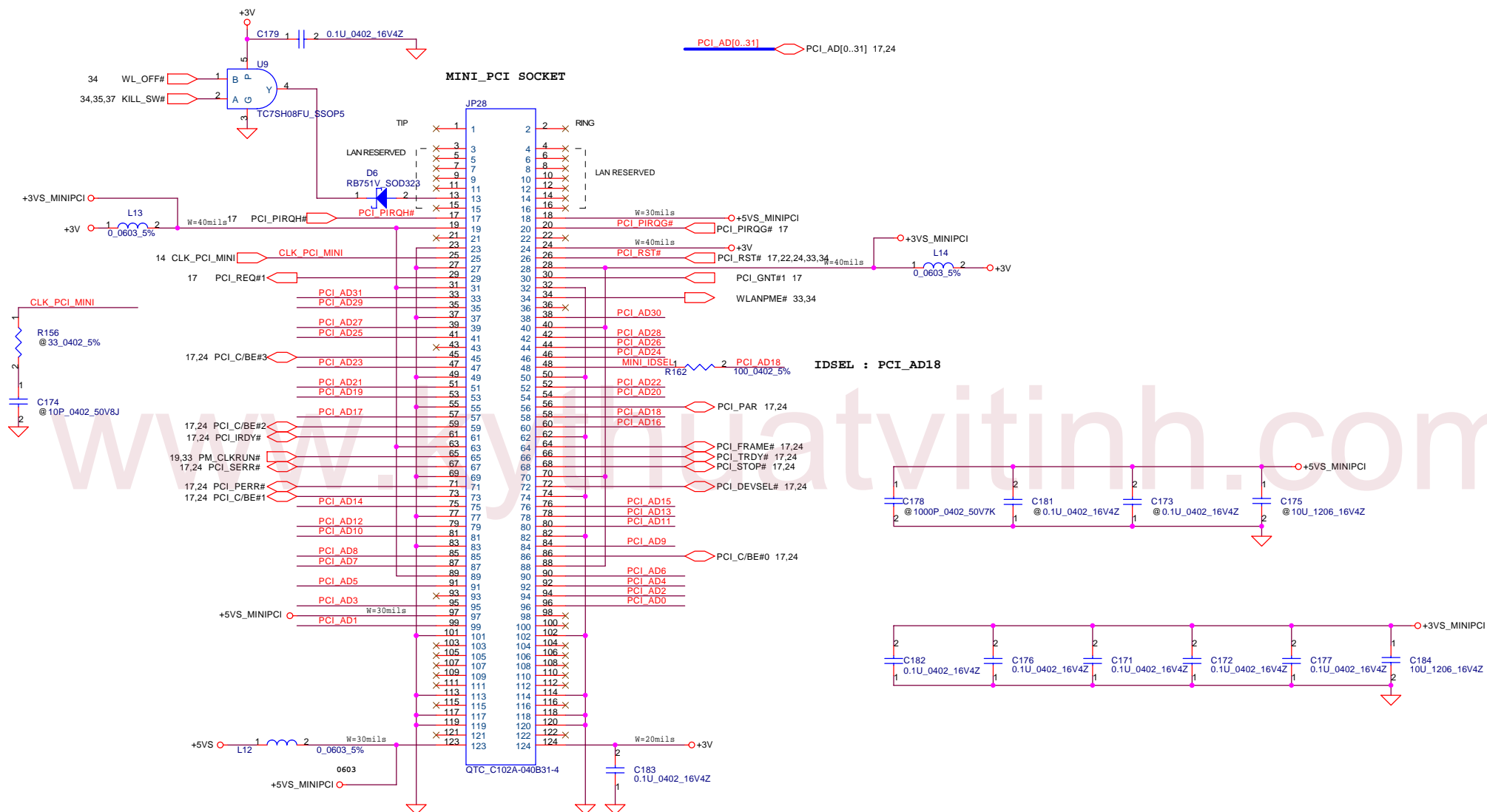
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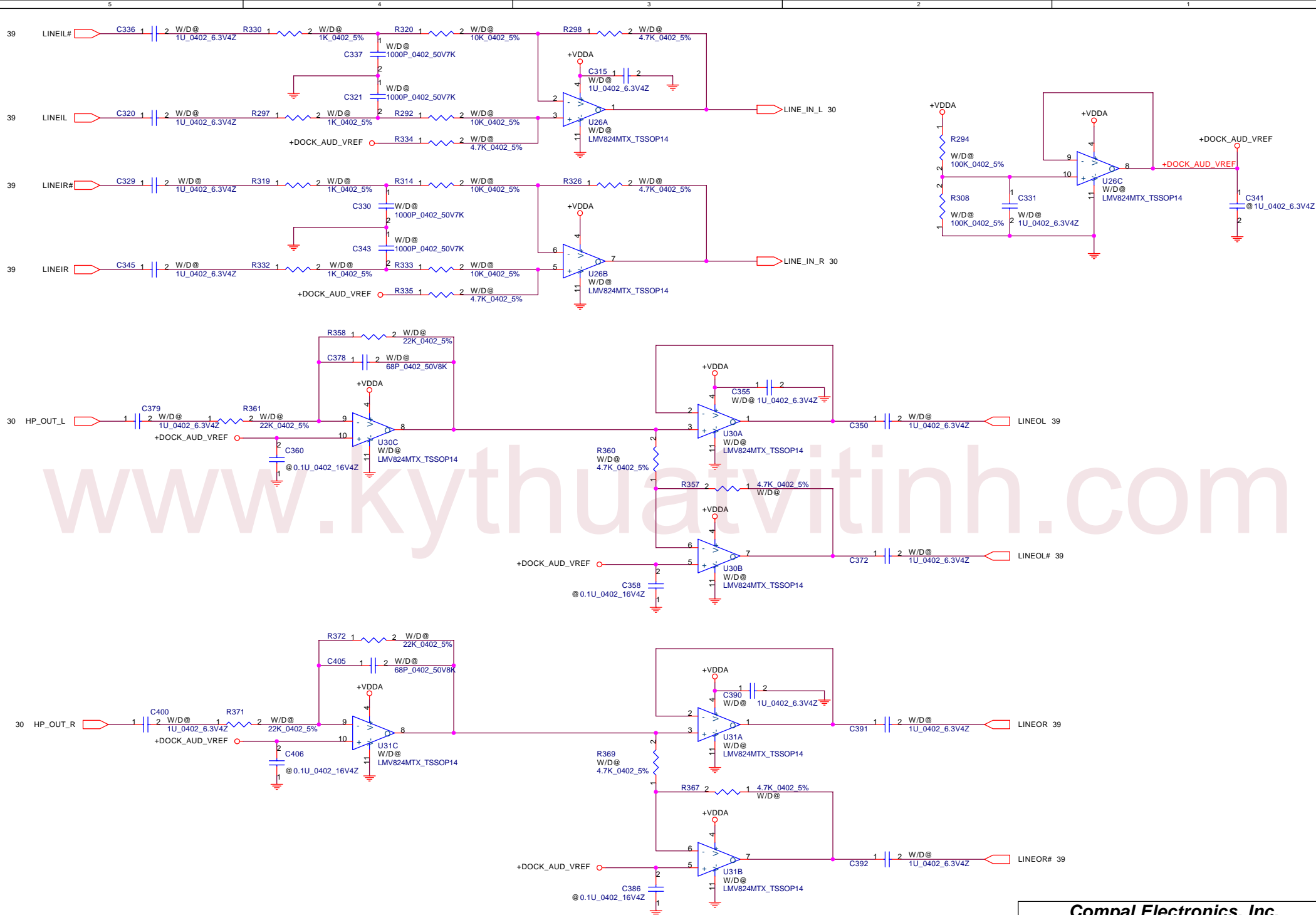
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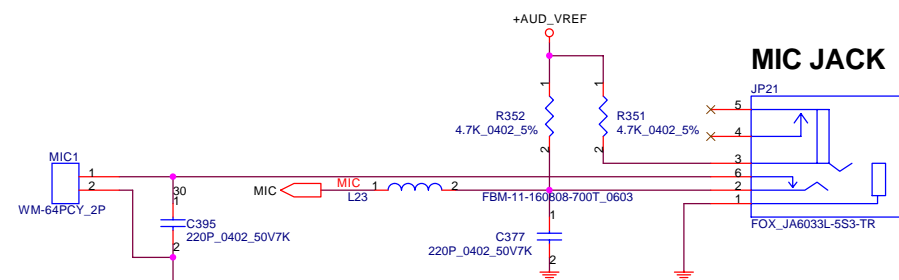
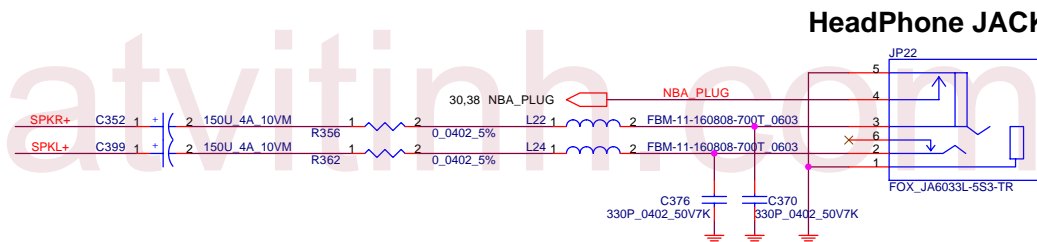
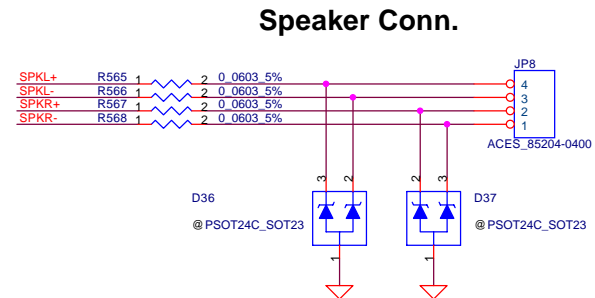
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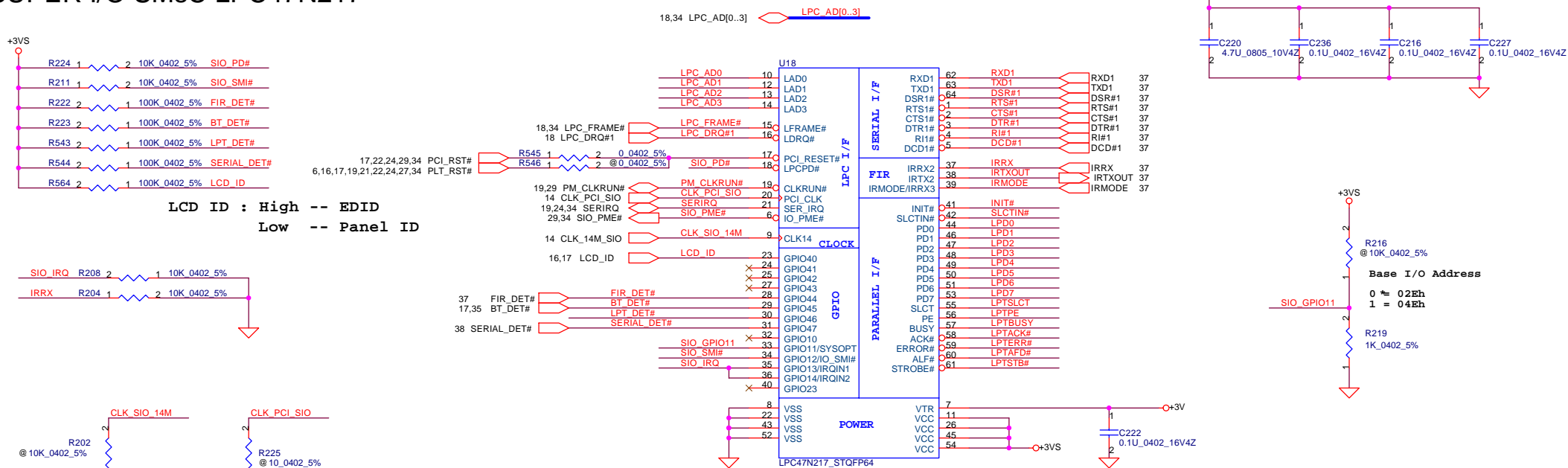
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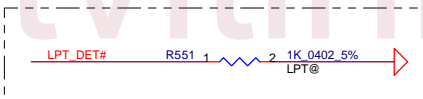
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SUPER I/O SMsC LPC47N217

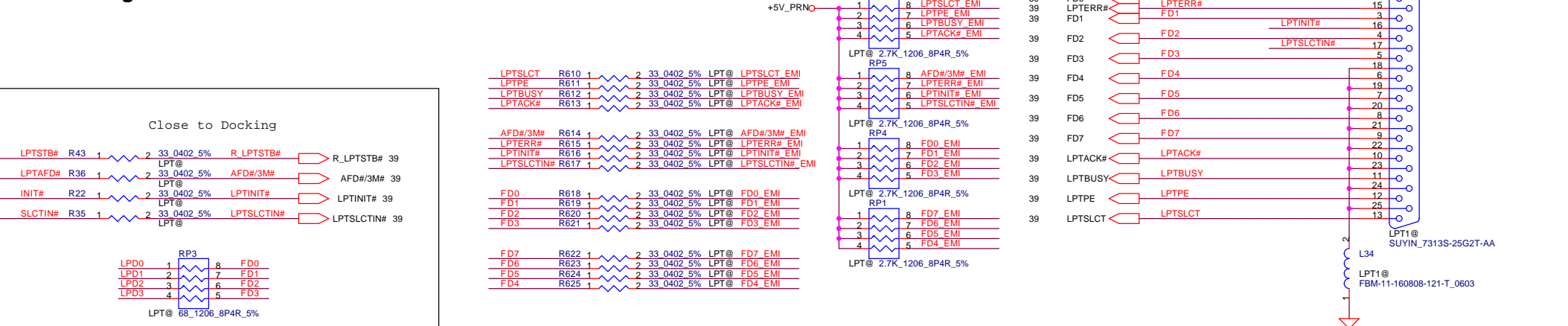


Parallel Port

LPT Module L: R POP LPT Enable
 H: R De-POP LPT Disable



No Docking and Parallel Port ----->Del



EMI Request for LPT ISSUE

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Compal Electronics, Inc.

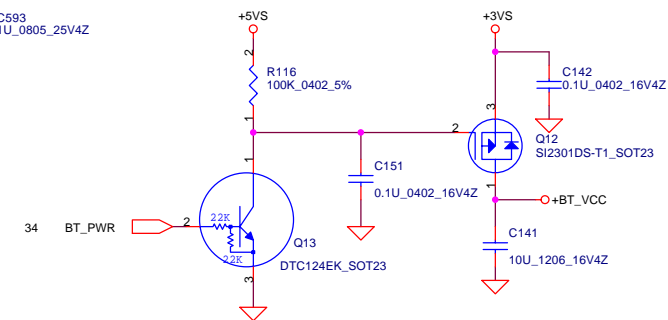
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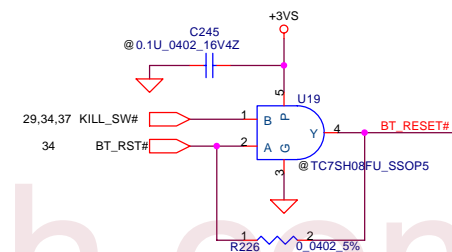
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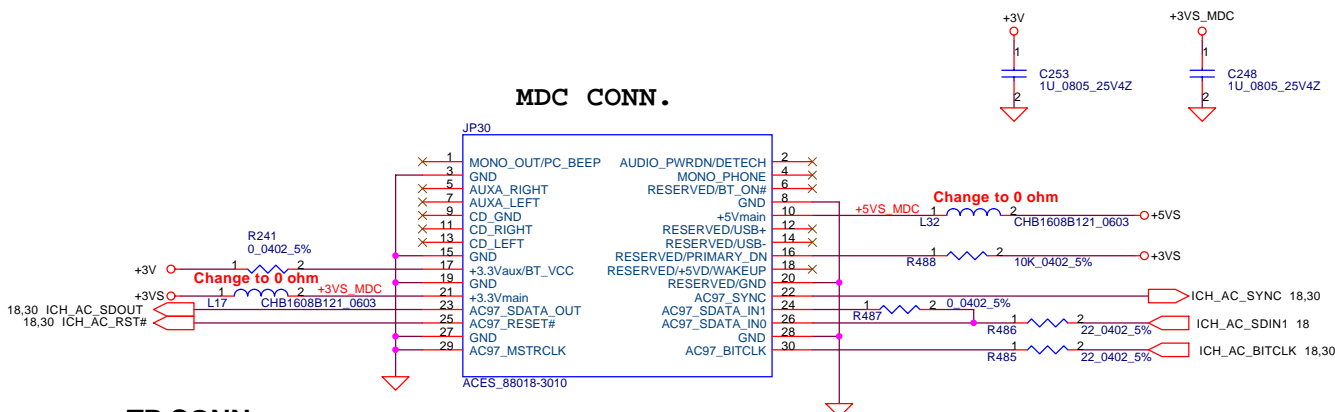
BlueTooth Interface



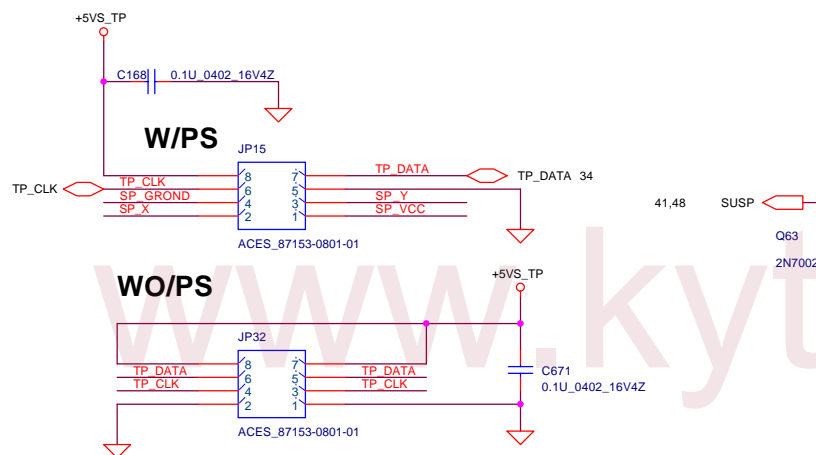
Module ID
Indication for polarity of reset
Reset input High Active --> Low
Reset input Low Active --> Open



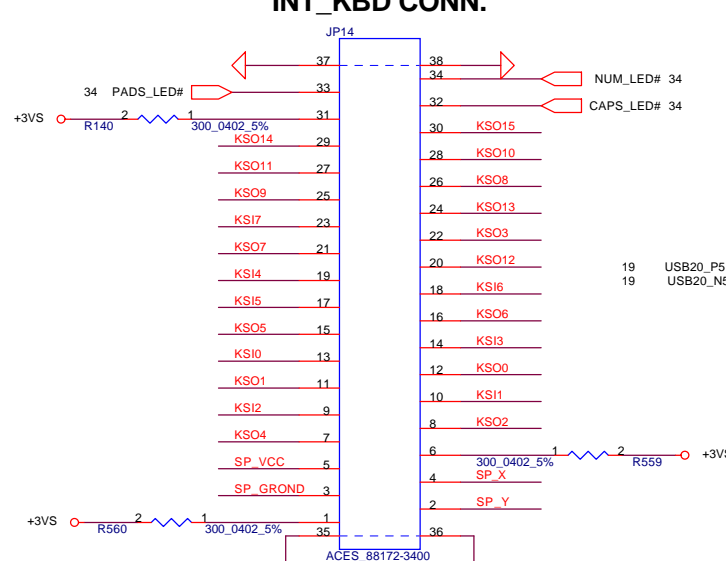
MDC CONN.



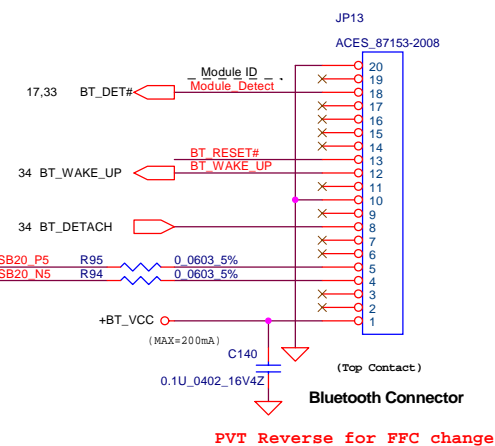
TP CONN.



INT_KBD CONN.



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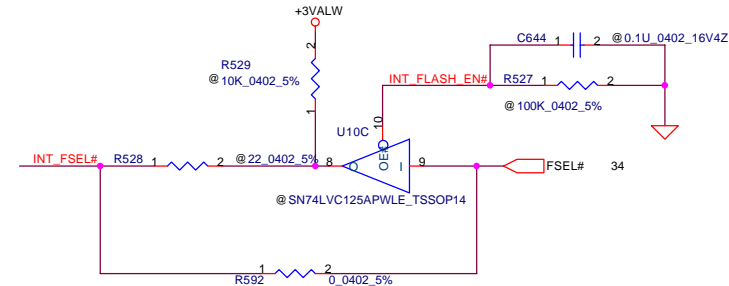
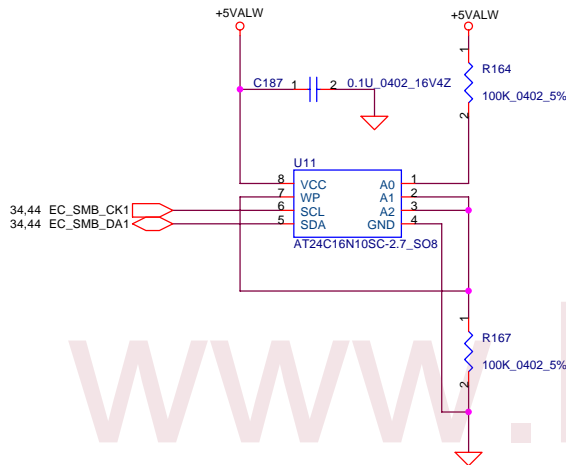
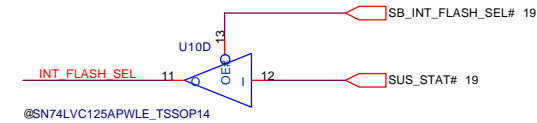
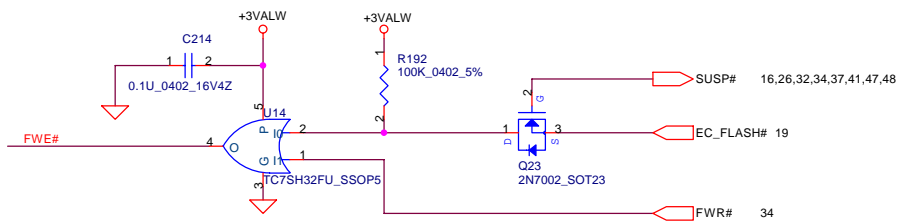


PVT Reverse for FFC change

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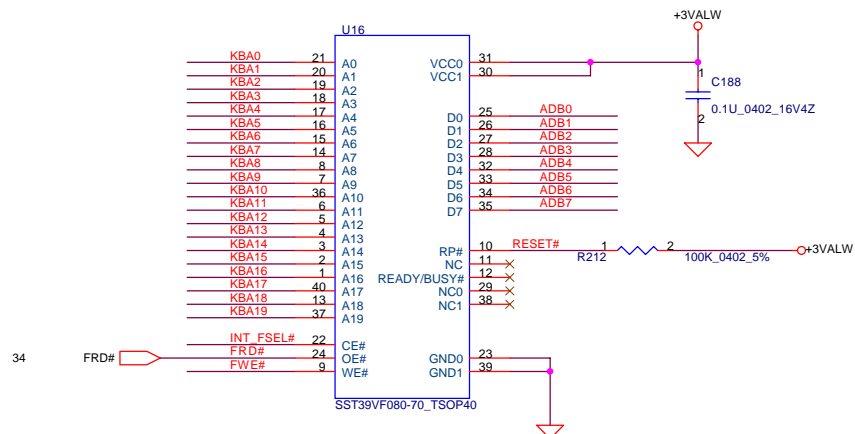
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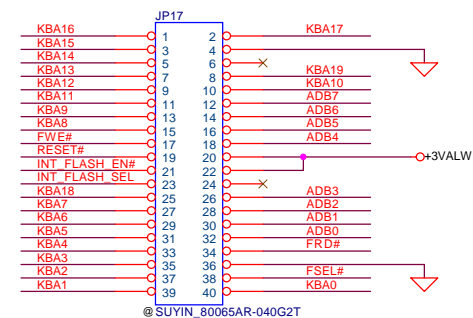


34 KBA[0..19] KBA[0..19]
34 ADB[0..7] ADB[0..7]

1MB Flash ROM



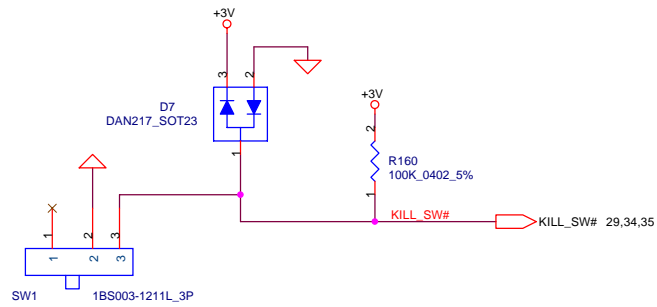
1MB ROM Socket



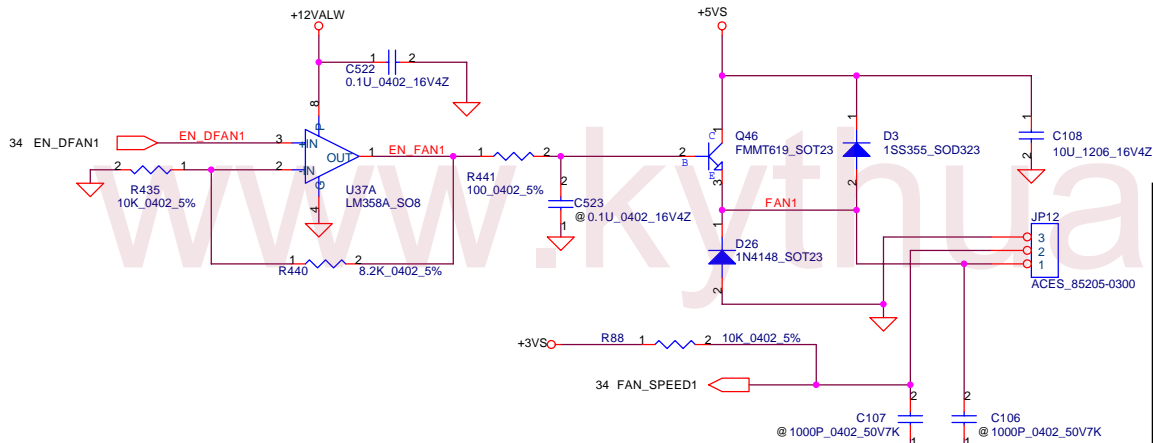
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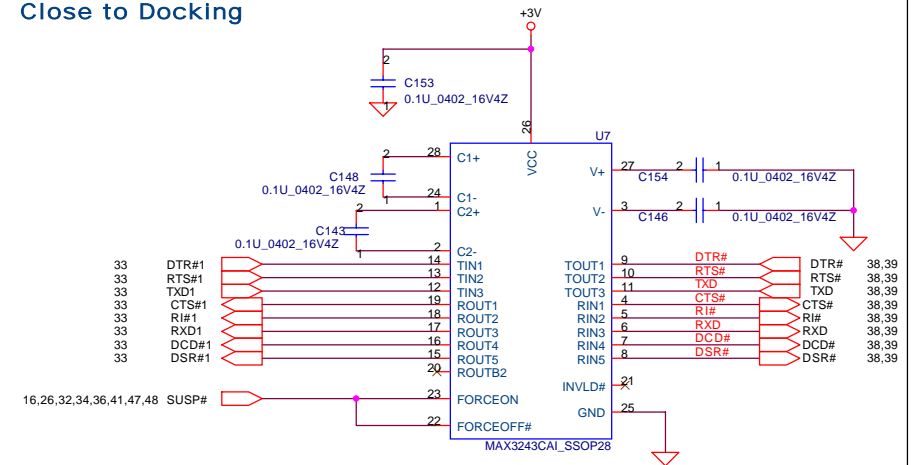
Kill SWITCH



FAN Conn



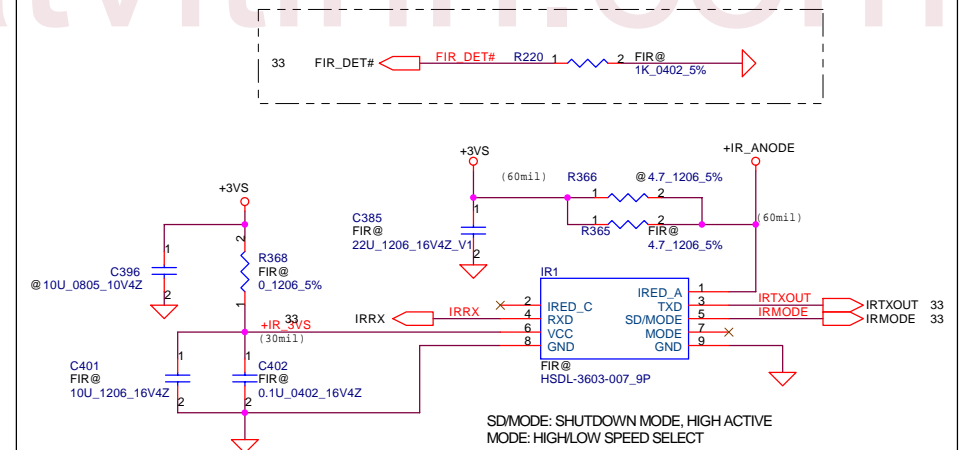
Close to Docking



No Docking and Serial Port ---->Del

FIR Module

L: R POP; FIR Enable
H: R De-POP; FIR Disable



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The diagram illustrates the wiring for the R4457 Serial Board. It features two main connection sections: USB20 and RJ45.

USB20 Connections:

- USB20_N7:** Connected to pin 30 of JP3.
- USB20_P7:** Connected to pin 29 of JP3.
- DTR#:** Connected to pin 28 of JP3.
- RTS#:** Connected to pin 27 of JP3.
- TXD:** Connected to pin 26 of JP3.
- CTS#:** Connected to pin 25 of JP3.
- RI#:** Connected to pin 24 of JP3.
- RXD:** Connected to pin 23 of JP3.
- DCD#:** Connected to pin 22 of JP3.
- DSR#:** Connected to pin 21 of JP3.
- SYSON#:** Connected to pin 20 of JP3.

RJ45 Connections:

- LAN_ACTIVITY#:** Connected to pin 15 of JP3.
- LAN_LINK#:** Connected to pin 14 of JP3.
- RJ45_GND:** Connected to pin 13 of JP3.
- RJ45_MD13+:** Connected to pin 12 of JP3.
- RJ45_MD13-:** Connected to pin 11 of JP3.
- RJ45_GND:** Connected to pin 10 of JP3.
- RJ45_MD12+:** Connected to pin 8 of JP3.
- RJ45_MD12-:** Connected to pin 7 of JP3.
- RJ45_GND:** Connected to pin 6 of JP3.
- RJ45_MD11+:** Connected to pin 5 of JP3.
- RJ45_MD11-:** Connected to pin 4 of JP3.
- RJ45_GND:** Connected to pin 3 of JP3.
- RJ45_MD10+:** Connected to pin 2 of JP3.
- RJ45_MD10-:** Connected to pin 1 of JP3.

Power and Grounding:

- +3VALW:** Connected to pin 30 of JP3.
- +5VALW:** Connected to pin 18 of JP3.
- 33 SERIAL_DET#:** Connected to pin 17 of JP3.
- 680P_0402_50V7K:** Two capacitors are shown, one connected to pin 16 of JP3 and another to pin 17 of JP3.

Pinout diagram for the ACES_87216-3002 module. The diagram shows a 30-pin connector with pins numbered 1 to 30. Pin 1 is labeled +5VALW. Pins 2-5 are labeled SYSON#. Pins 6-9 are labeled USB_OC#0, USB_OC#2, and USB_OC#4. Pins 10-11 are labeled NBA_PLUG and VOL_AMP. Pins 12-15 are labeled VOL_AMP. Pins 16-19 are labeled USB20_N0, USB20_P0, USB20_N2, and USB20_P2. Pins 20-23 are labeled USB20_N4, USB20_P4, and LID. Pins 24-25 are labeled RTCVREF and +5VCD. Pins 26-29 are labeled NBA_PLUG and VOL_AMP. Pins 30-32 are labeled NBA_PLUG and VOL_AMP. The diagram also shows connections to a USB20 module and a RTC module.

The schematic diagram illustrates the battery status indicator circuit. It consists of two NPN transistors, DTC115EKA_SOT23 Q20 and DTC115EKA_SOT23 Q51, configured as comparators. The non-inverting inputs of Q20 and Q51 are connected to the BATT_CHGLED# and BATT_LOWLED# signals through 200_0402_5% resistors (R163 and R471). The inverting inputs of Q20 and Q51 are connected to the same signals through a 100K resistor and a 100K feedback resistor. The outputs of Q20 and Q51 are connected to the BATT_CHG_LED# and BATT_LOW_LED# pins. The circuit is powered by a 3.3V supply.

[illegible]

Pin 17: HT-191NB_BLUE_0603

AC IN LED

5VALW

R364 120_0402_5%

D18 HT-191NB_BLUE_0603

19.34,43 ACIN

Q40 2N7002_SOT23

HT-297UD/NB_BLUE/AMB_0603

MODE

+5VS

R376

1 2

@ 120_0402_5%

D19

@ HT-191NB_BLUE_0603

1 2

MODE_LED# 34

WL LE

0.4143 VALW

R370

1

2

300_0402_5%

2

1

D15

HT-110UD_1204

WL_BT_LED# 34

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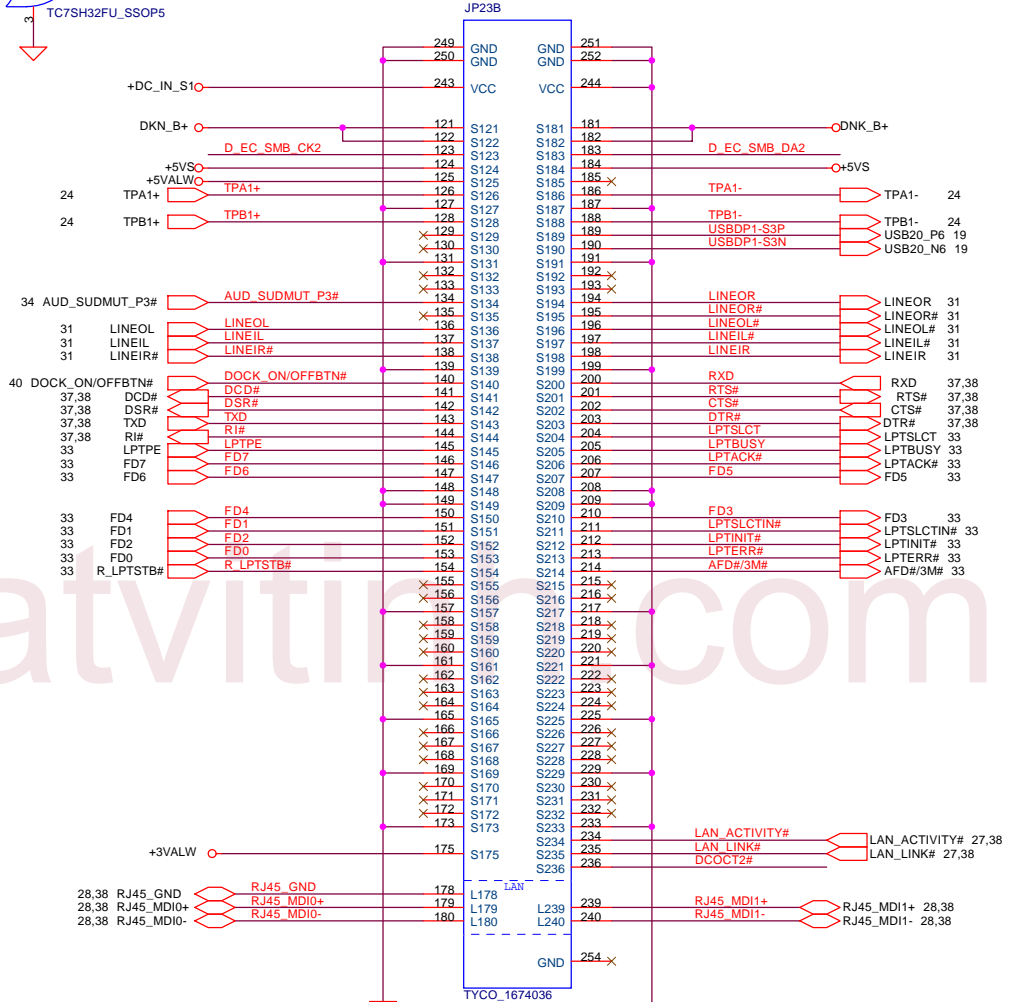
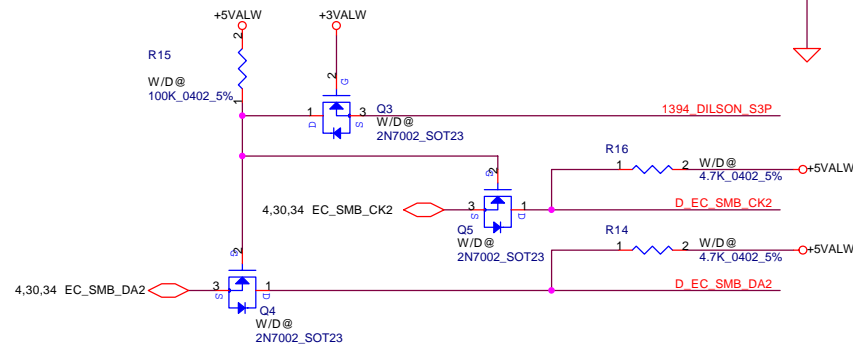
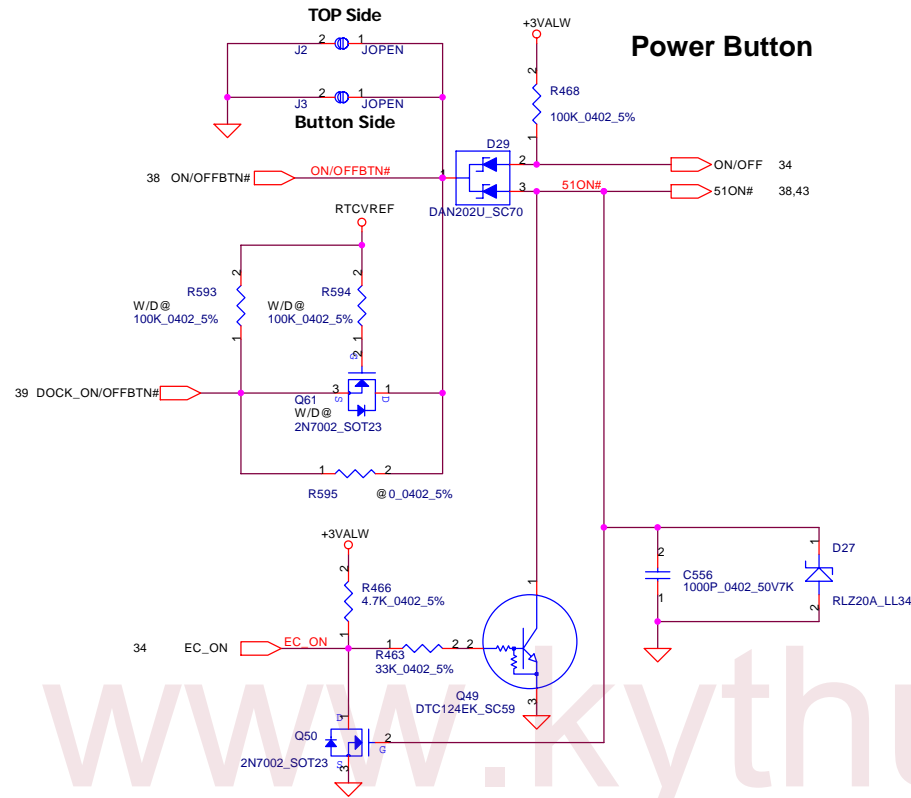


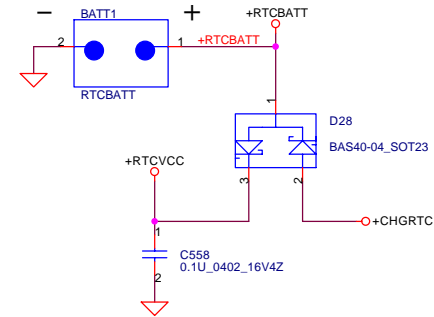
Diagram showing the connection of MDC1 RING and MDC2 TIP to the JP2 connector. The MDC1 RING is connected to pin 1, and the MDC2 TIP is connected to pin 2. The connector is labeled JP2 and W/D@ ACES_85205-0400.



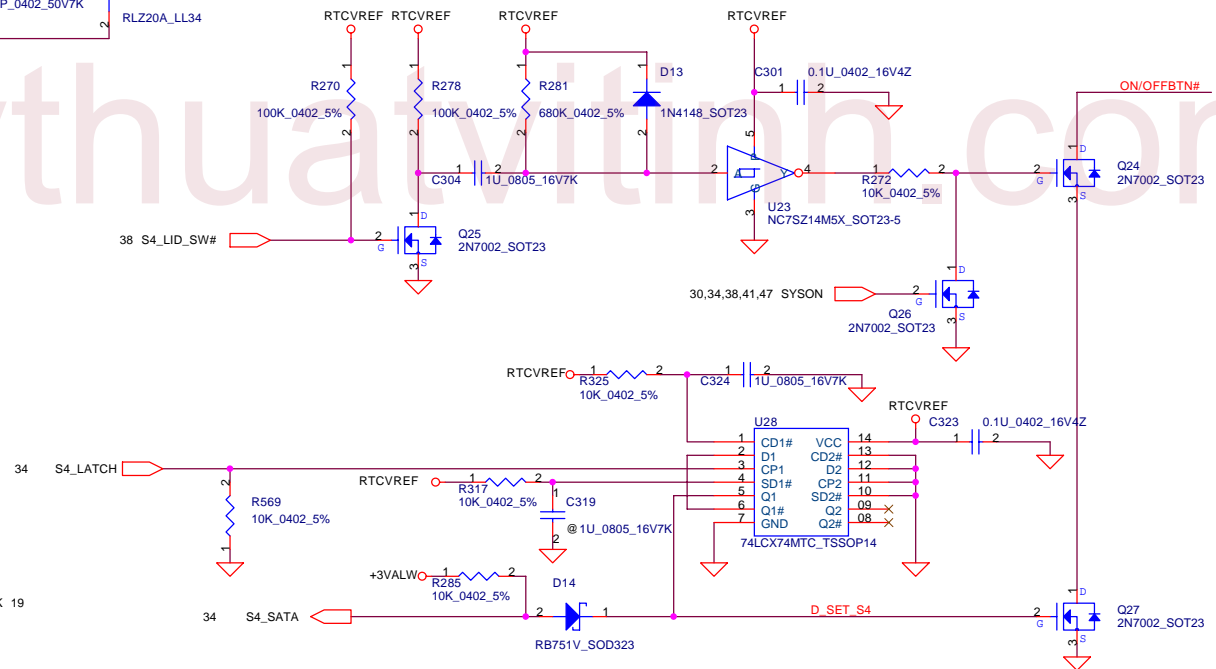
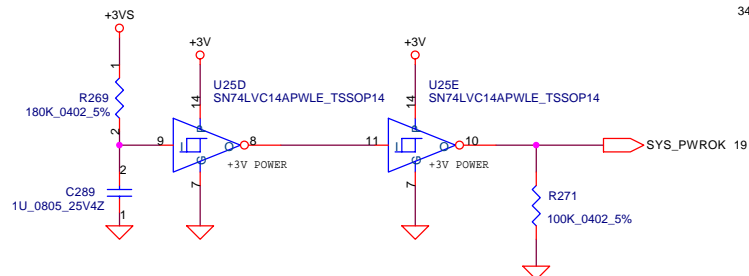
Power Button



RTC Battery

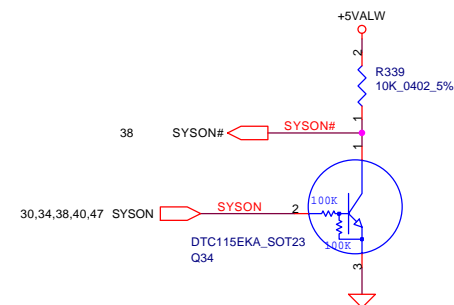
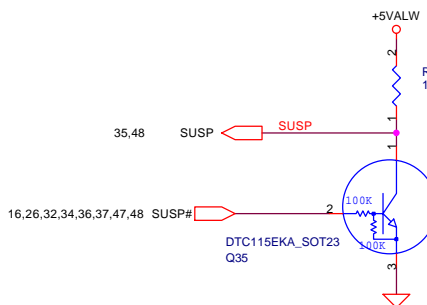
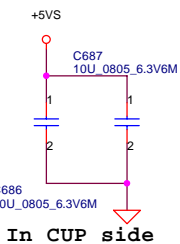
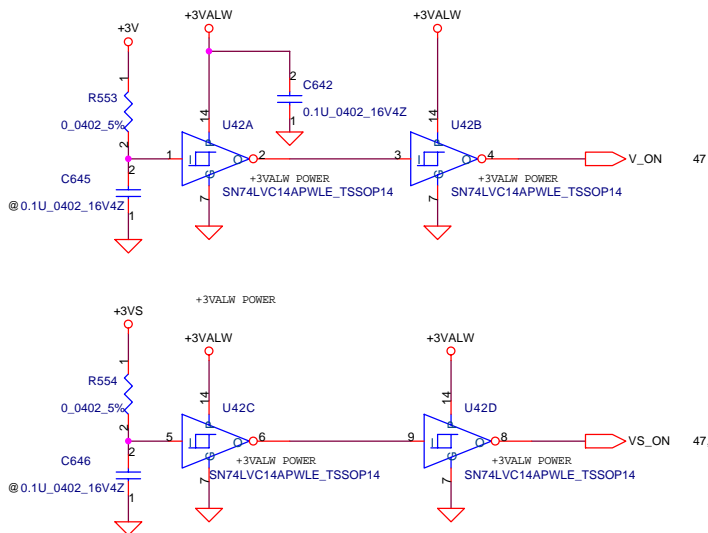
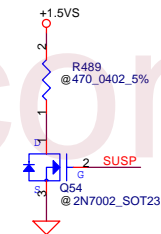
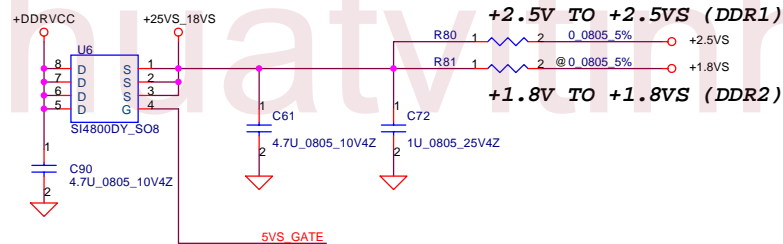
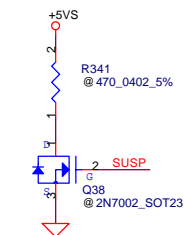
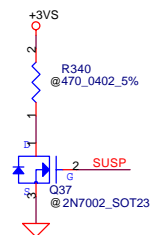
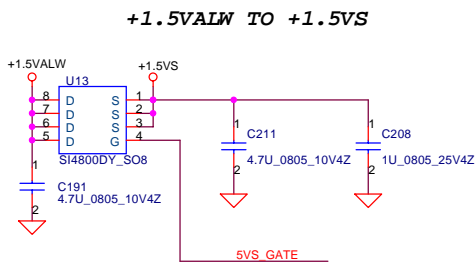
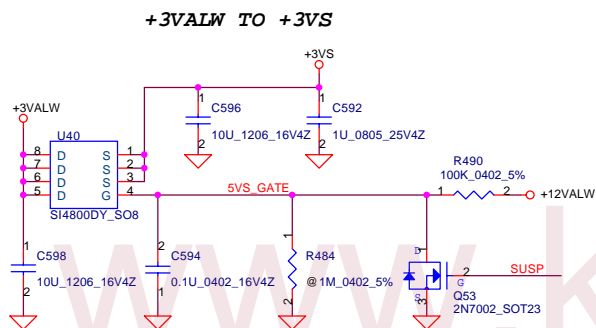
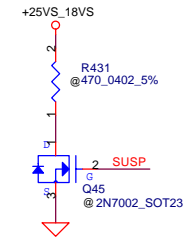
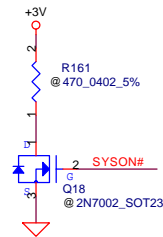
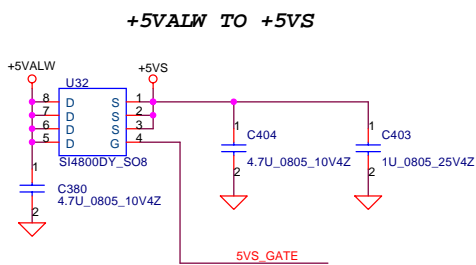
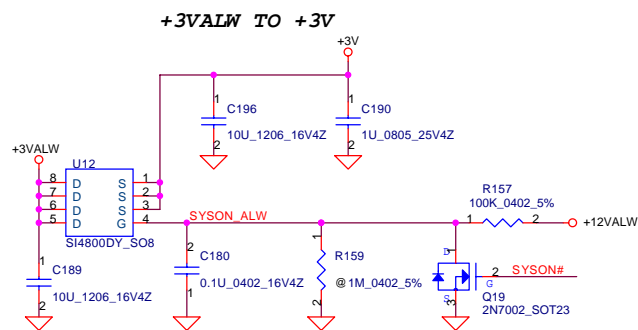


Power ON Circuit



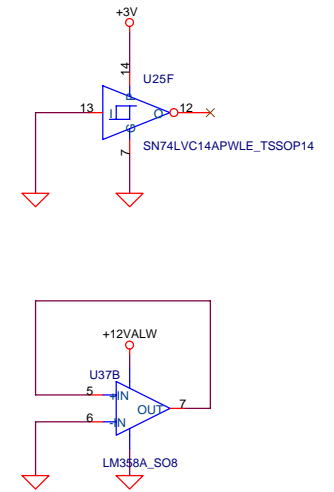
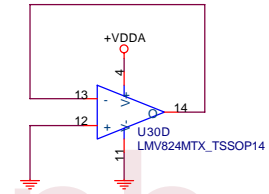
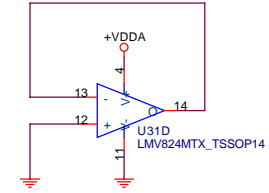
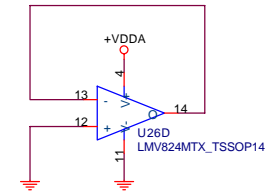
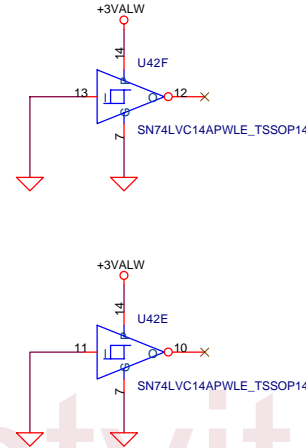
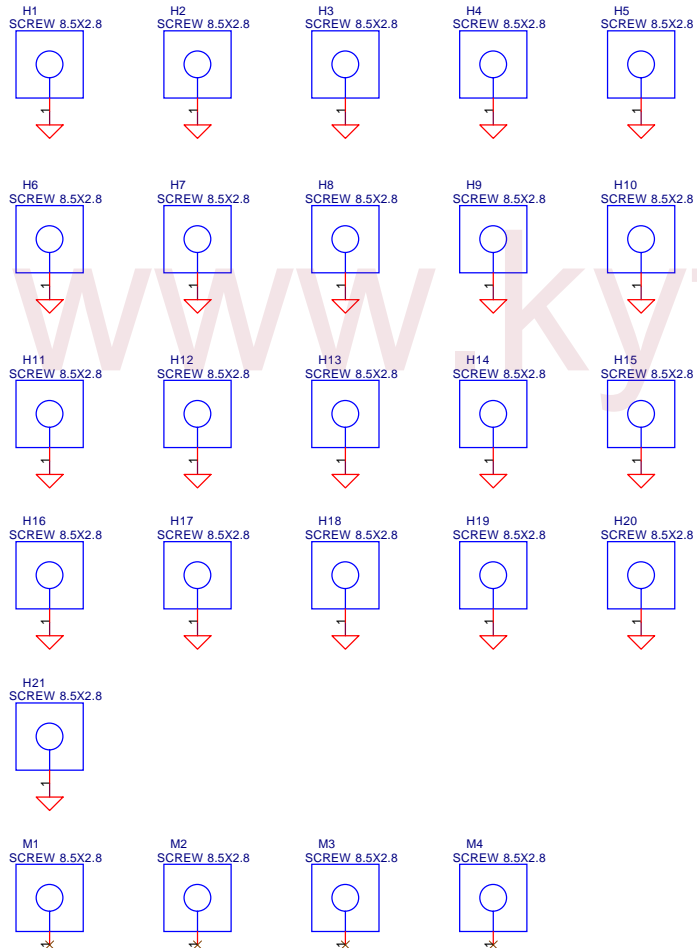
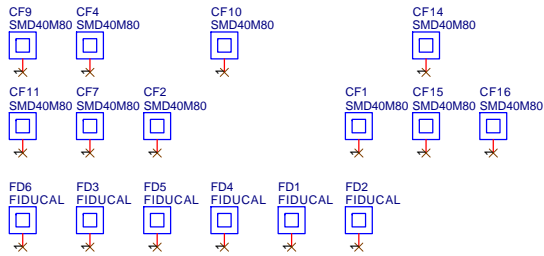
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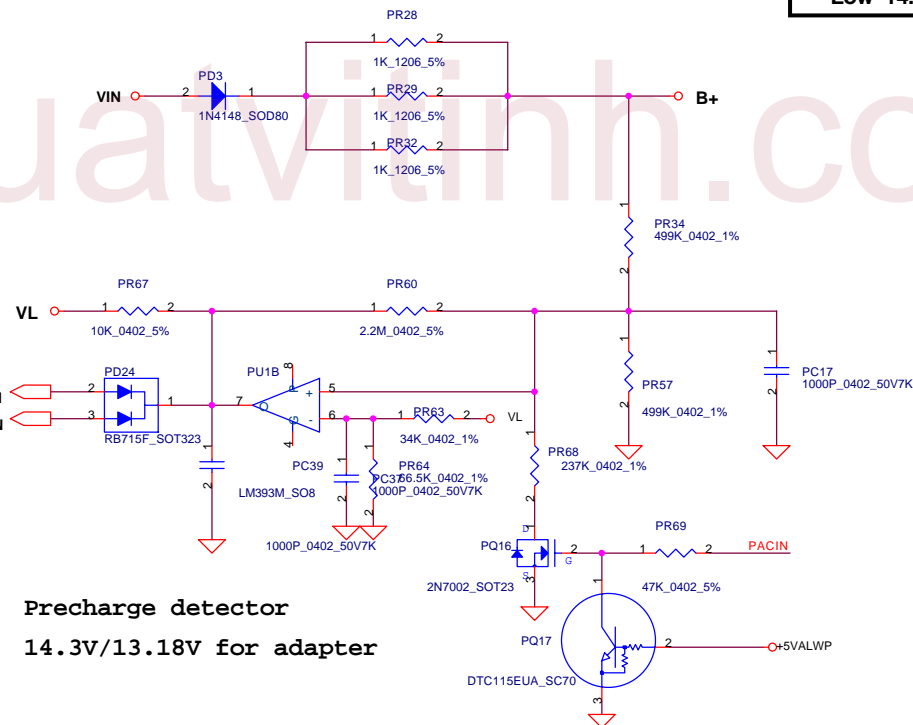
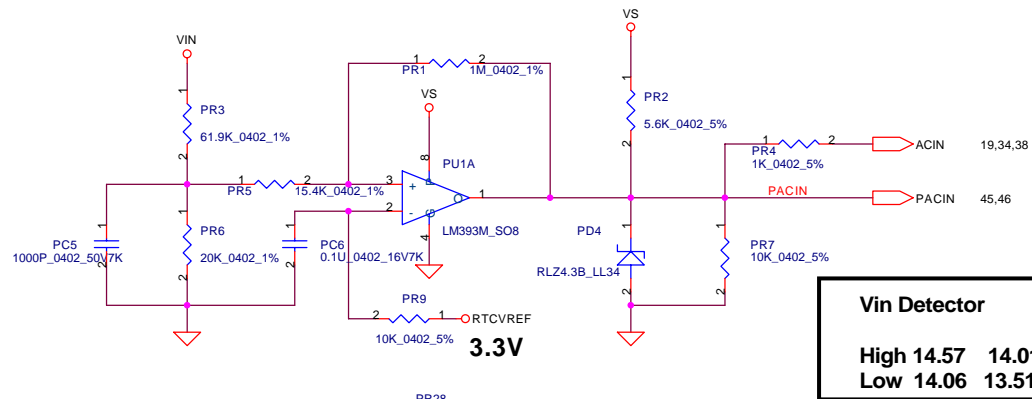
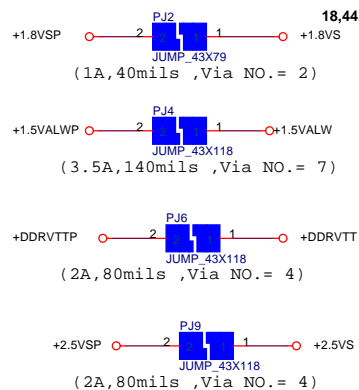
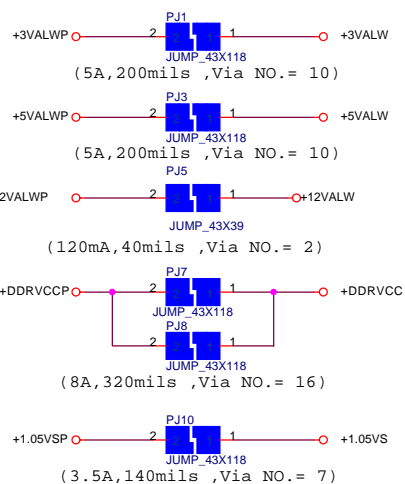
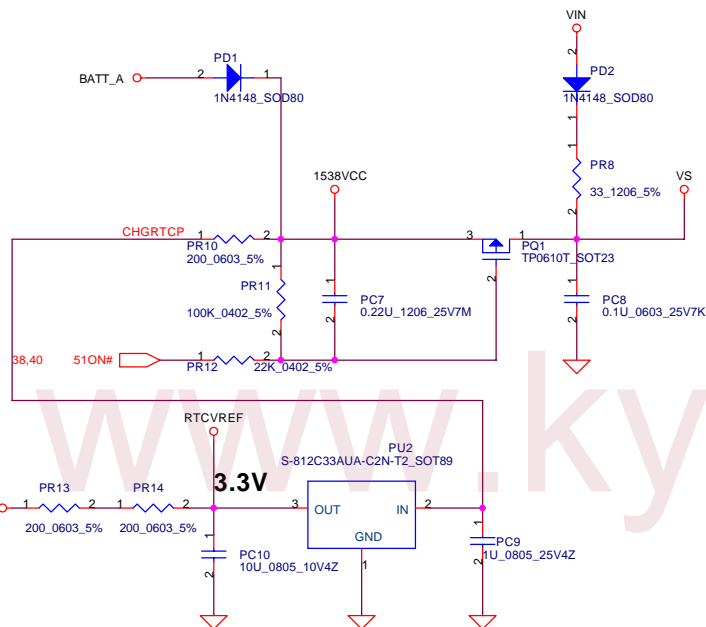
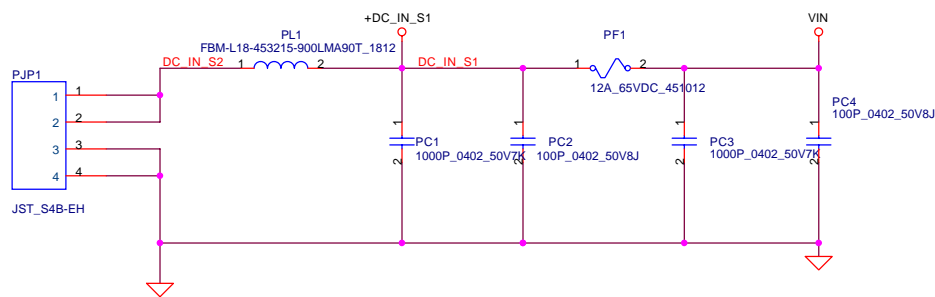


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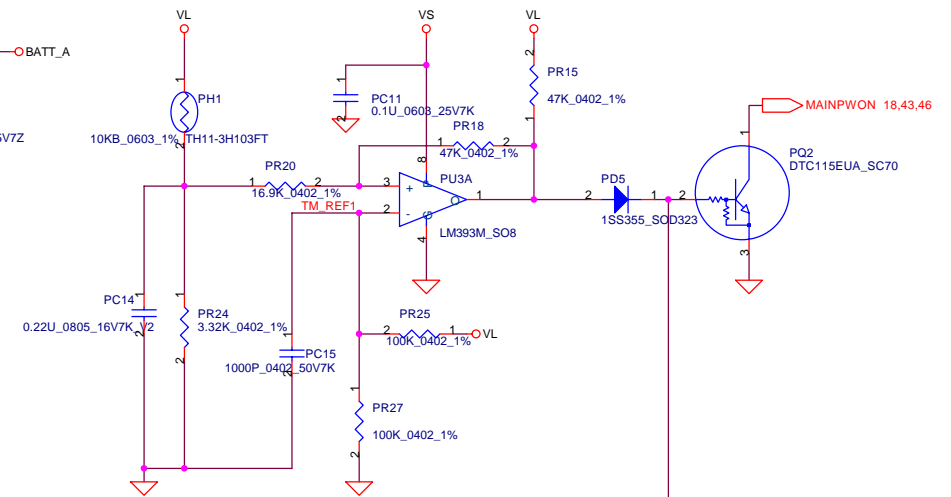
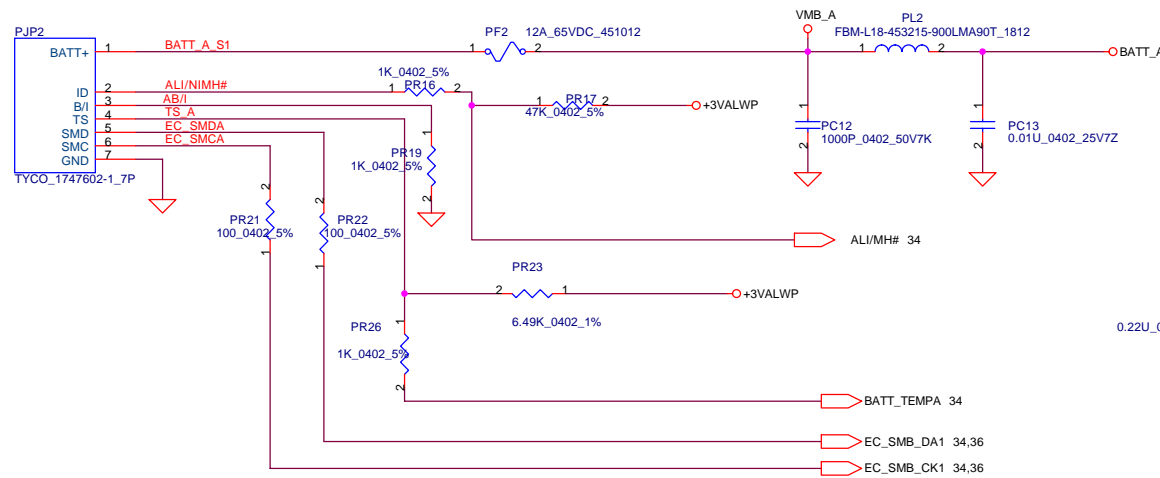


Precharge detector
14.3V/13.18V for adapter

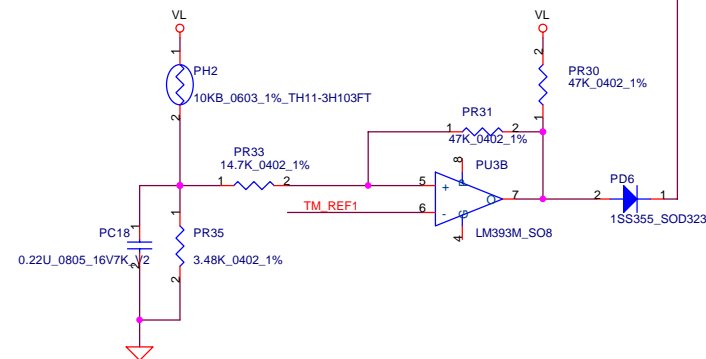
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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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$I_{adp}=0-4.7A$

$CC=0.5-3.3A$
 $CV=12.6V(9\text{ CELLS LI-ION})$

$I_{REF}=1.31 \cdot I_{charge}$
 $I_{REF}=0.6V \sim 3.21V$

+3VALWP

4.2V

OVP voltage : LI
3S3P : 13.5V--> BATT_OVP= 1.5V
(BATT_OVP=0.1111 *VMB)

34 BATT_AOVP

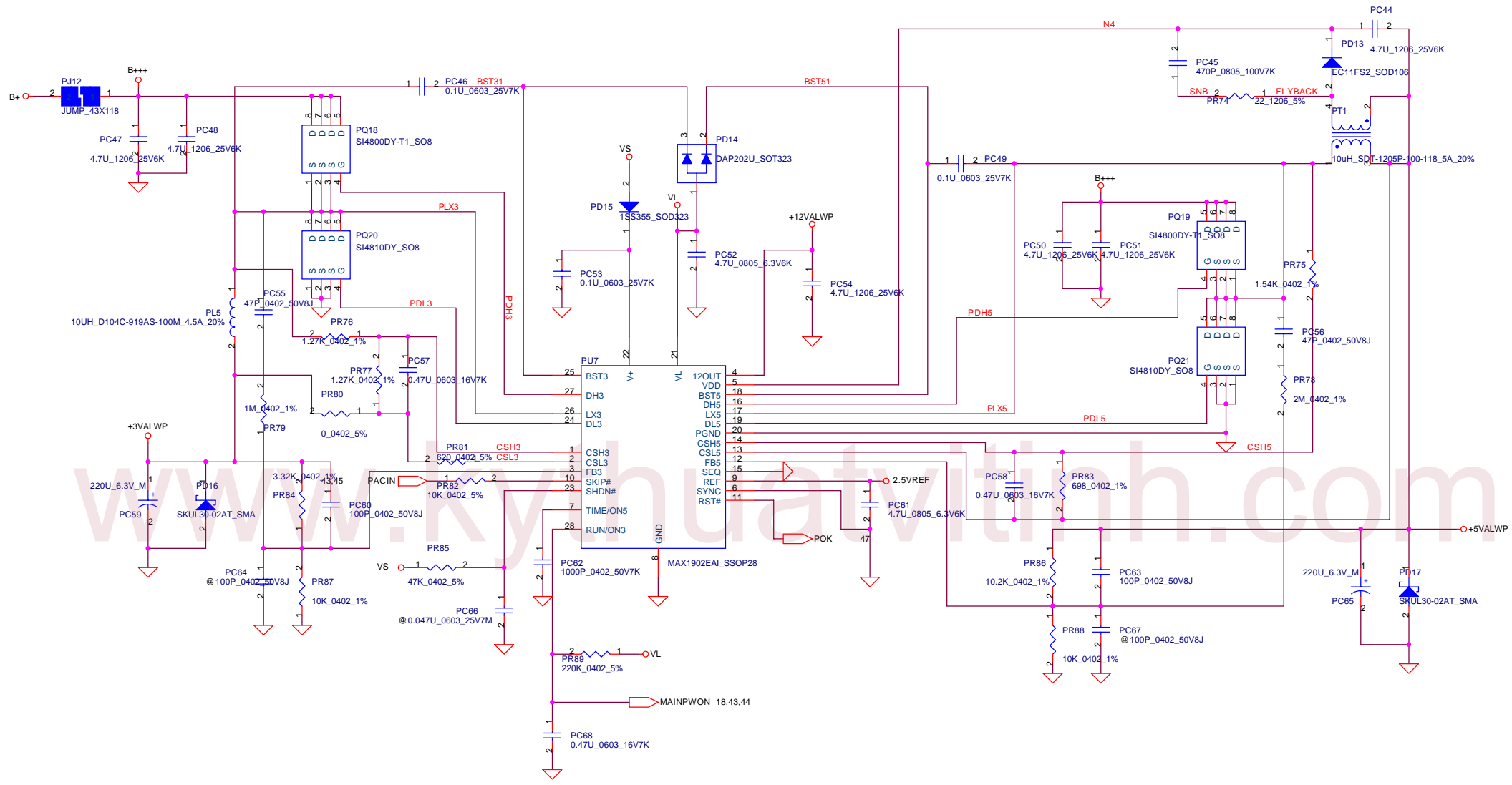
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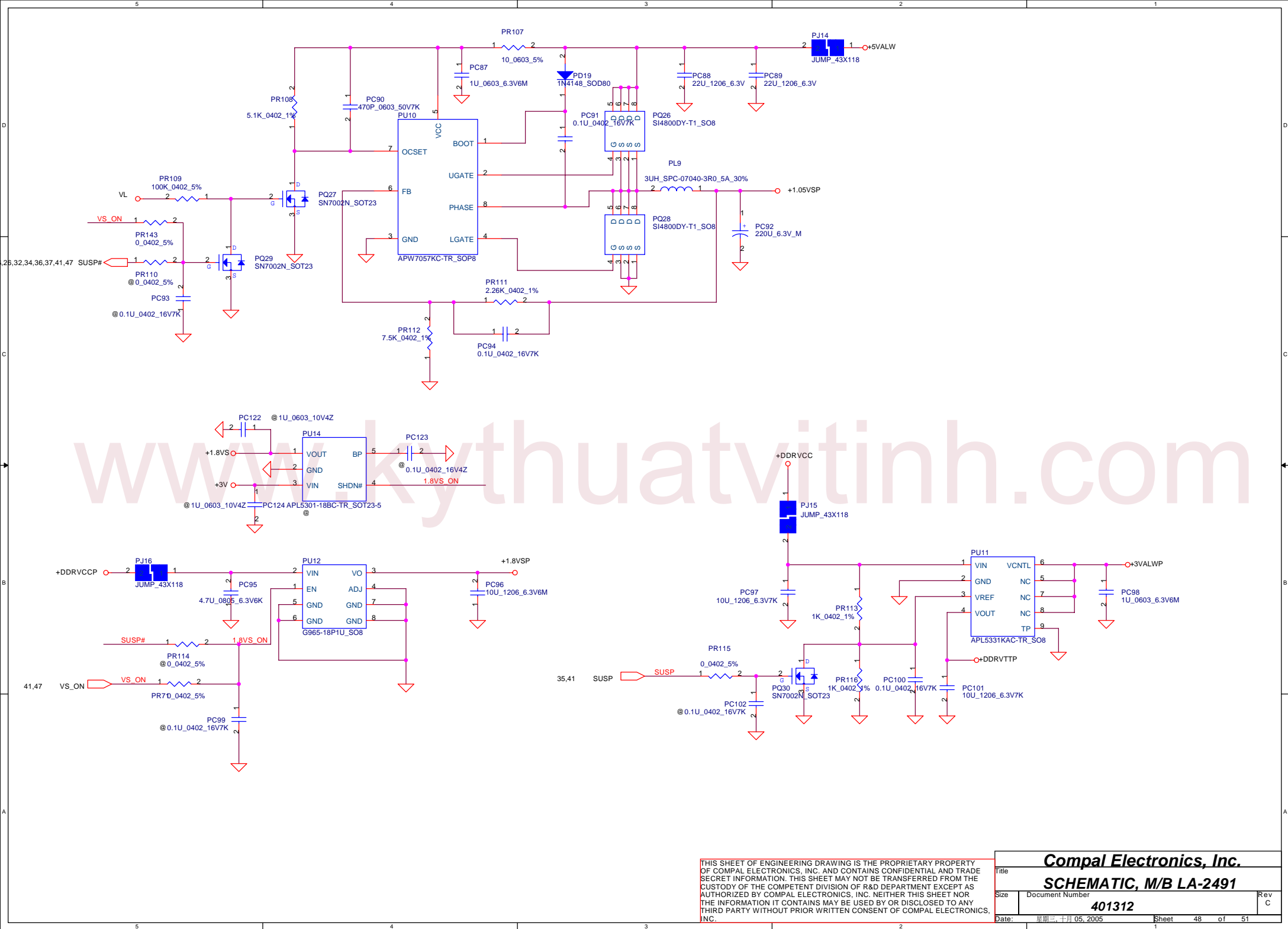
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EAT10 PIR List

***** Rev:0.2 PIR List 2004/08/10 Writer by Jason *****

P05:Add @ in R63
Del @ in R56

P06:Del @ in R54
Del JP9

P08:Q6, Q43, Q44 Horizontally
*GMCH_TXCLK-, GMCH_TXCLK+ Swap

P12:+3VS change from JP25.194 to JP25.196

P15:Update U4 CIS lib

P16:Del JP9
New add Q56

P21:New add R513
New add X3
New add C607

P22:New add R514, R534, @R535

P30:New add C639, C640
Change U27 to ALC250D
New add @R539, @R540, @R542, @Q59
New add @R536, @R537, @R538, @R541, @Q58
New add C608, C609, R522, R521, R526, C610, C611, C612, C641, X4
New add @R523, @R524, @R525
Del R295, R296, R310, R327, L20, @C311, C374

P33:New add R543, R544

P34:Del @ in R478
New add R547, @R548, R549, R550

P35:Del CP2, CP3, CP4, CP5, CP6, CP7
Modify JP14 Pin Define
New add C613, C614, C615, C616, C617
New add C618, C619, C620, C621, C622
New add C623, C624, C625, C626, C627
New add C628, C629, C630, C631, C632
New add C633, C634, C635, C636

P36:Del @U42, @C608
New add U43, U44, U45
New add C637, C638
New add R527, R528, R529

P37:Swap JP12.1, JP12.3
Swap SW1.1, SW1.3

P38:Q52 change from 2N7002 to DTA114
New add R530, R531, R532, R533, Q57

***** Rev:0.3 PIR List 2004/10/26 Writer by Sam Tsai *****

P04:Add @ in R28 Intel Recommend

P06:Add @ in C441, C427
~~DT2789~~ C460 Change Value from 220U to 330U Power Team testing OK

P12:+3VS change from JP25.196 to JP25.194 Intel Recommend

P15:New add R570, R571 & R572 RGB without Docking
New add L33 EMI
Del D2 & D25

P16:Change U44 from 7404 to 74125 LCD/VDD Soft-Start

P18:New add R573 Intel Recommend
R439 Change Value from 180K to 20K Intel Recommend
C271 Change Value from 0.1U to 1U Intel Recommend

P20:R214 Change Value from 1K to 10ohm Intel Recommend

P22:New add @R , @R& Q SWDJ testing

P24:New add R586 TI Recommend
New add @R581

P25:New add R582, R583, @R584, R585, R588, R589 & @C685 TI Recommend

P27:R73 Change Value from 4.99K to 4.7K Marvlll Recommend

P31:R361 & R371 Change Value from 47K to 22K Design Change

P33:New add R543, R544 Design Change

P32:Modify C399 Net to SPKL+

P33:New add L34 EMI
add@ in C647 ~ C662

P34:New add R587 Design Change

P35:New add JP32 & C671 Design Change
New add C682 ~ C684 EMI
JP13 reverse Design Change

P36:New add SWDJ testing

P37:SW1 change to 1BS003-1211L_3P Design Change

P38:Q52.3 change from +3VALW to +3V Design Change
Q57.3 change from +5VALW to +5VS
Lid Switch IC Power change from JP16.26 +3VALW to JP16.27 RTC/VREF
New add C672 ~ C681 EMI

P39:New add R574 Design Change

P40:Del D11 Design Change

***** Rev:1.0 PIR List 2004/12/12 Writer by Sam Tsai *****

P06:Add @ in R426 and R427 Intel Recommend

P09:Add C689, L35 Tv Wave Issue

P19:New add R597 Intel Recommend

P21: Add R604 SWDJ reserve

P21: Add R590, R591 PJ17 SWDJ reserve

P24:New add R598, @R599, R600, @R601 TI Recommend
New add C691 TI Recommend-4510

P25:New add R602, @R603 TI Recommend

P34:SWAP PIN25 & PIN88 Design Change
R178 Change Value from 100K to 470

P35: Add Q62, Q63, Q64 , R605, R606, R607, @R608, C690 Design Change

P36: Add R592 Design Change

P38: Add R609, D35 Design Change

P41: Add C686, C687 Design Change

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Version Change List (P. I. R. List) for Power Circuit

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